Built-in Current Sensor for IDDQ Test

Bin Xue D. M. H. Walker

Dept. of Computer Science
Texas A&M University
College Station TX 77843-3112
Tel: (979) 862-4387
Fax: (979) 847-8578
Email: walker@cs.tamu.edu

Abstract

A practical Built-in Current Sensor (BICS) design is described in this paper. This sensor system is able to monitor the IDDQ at a resolution level of 10 μA. This system can translate the current level into a digital signal, with scan chain readout. There is no system performance degradation for this sensor and its power dissipation is kept at a very low level. With the help of a self-calibration circuit, the sensor can maintain its accuracy and achieve a clock rate of over 1 GHz, for a measurement time of a few milliseconds.

1. Introduction

Quiescent current (IDDQ) testing can screen out many defects that escape other test methods [1][2]. It is also very useful in defect diagnosis [3]. However the future of IDDQ testing is uncertain. The International Technology Roadmap for Semiconductors projects that IDDQ levels will rise rapidly with each technology advance [4][5]. Built-in current sensors (BICS) have been proposed both to speed up IDDQ testing and to increase its resolution by virtually partitioning the supply mesh, so that each partition has a relatively small defect-free IDDQ level [6]. However all BICS designs proposed to date have unacceptable drawbacks, including large area overhead, chip speed penalty, high power supply voltage, substrate current injection, or limited BICS locations [7][8][9][10]. As a result, BICSs have rarely been used in production. Our previous work using a MAGFET sensor in a BICS had unacceptable noise level and calibration drift [11]. In view of these shortcomings, we propose a new BICS design, which has the advantage of small area overhead, no chip speed penalty and it can be used for practical IDDQ testing and diagnosis of large, high-performance chips through the 32 nm technology node.

2. Description

We have developed a prototype BICS that measures the very small voltage drop along a segment of the supply network of the circuit under test and monitors the IDDQ that causes this voltage drop. This avoids any chip performance penalty since no series impedance is placed in the supply network. The BICS consumes very little power during testing and no power when testing is finished. The signal is digitized using a self-calibrated stochastic sensor, which is read out via a scan chain. The BICS is small, fast, low-power, high resolution, and can be used in large numbers on a chip [12]. The block diagram of the BICS is shown in Figure 1. The major BICS components are the flip-flop sensor, calibration circuit, and counter/scan chain. The prototype design has been fabricated in the MOSIS 1.5μm AMI process.

The BICS system works as follows. The signal, a small voltage drop from the supply line, passes through the transmission circuit and into the stochastic sensor. The signal strength is decided by the supply line length and resistance. Ten squares of supply line will generate a 1 μV signal when the current is 10 μA and the sheet resistance is 10 mΩ/□. The stochastic sensor amplifies the small signal and resolves into either "1" or "0" in each clock cycle. The probability of the stochastic sensor resolving into each state is determined by the signal to noise ratio (SNR). The generated bit stream of "0" and "1" is then fed into the counter, where it is accumulated. A self-calibration circuit nulls out any flip-flop imbalance and layout mismatch when no input signal is present. The signal is removed for calibration by opening the transmission circuit and shorting the stochastic sensor inputs. The flip-flop sensor achieves high sensitivity by operating in the metastable region [13]. It compares the input signal to random noise to determine which way to flip. The data detector converts this flip to a counter clock pulse. The counter value is the digital representation of the signal, so the stochastic sensor plus counter form an analog to digital converter (ADC). The counter value can then be scanned out. The stochastic method has two advantages: an ADC can be implemented in a small area using digital components, and it can measure a signal much smaller than the random noise. The function of each block is explained in the following sections.

2.1. Transmission Circuit

The transmission circuit plays two roles. In measurement mode it passes the voltage signal from the supply line to the flip-flop stochastic sensor. In calibration mode, the circuit stops sampling the supply and shorts the

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2 inputs of the flip-flop sensor. This design ensures there is no performance degradation of the circuit under test since there is no series impedance on the supply line. The detailed circuit is shown in Figure 2. As shown, this transmission circuit taps off a supply line (the supply line is not shown) at two points ina/inb with pass transistors P0/P1 and feeds the flip-flop stochastic sensor at two outputs outa/outb. Small capacitors on these output nodes form low-pass filters in combination with P0 and P1 to reject high-frequency supply noise. NMOS transistors N0/N1 were used as capacitors by tying their source, drain and bulk together. The pass transistors P0/P1 are turned off and outputs are clamped to Vdd by P4/P5 during the calibration cycle. PMOS transistor P3 is used to remove any imbalance between the two output nodes. This permits calibration immediately prior to sensing, greatly reducing the drift requirements of the calibration circuit. The devices are larger than the technology minimum size to reduce mismatch and noise. The circuit in Figure 2 is designed to sense the Vdd line, but can be readily redesigned to sense the ground line. Sensing both Vdd and ground can reduce the number of sensors required [12].

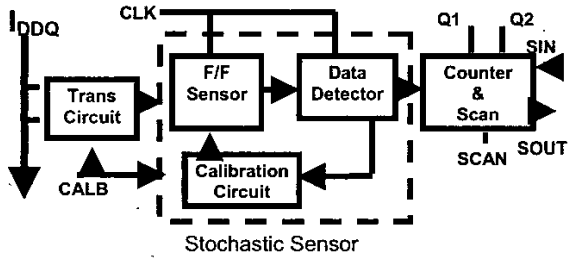

Figure 1. BICS block diagram

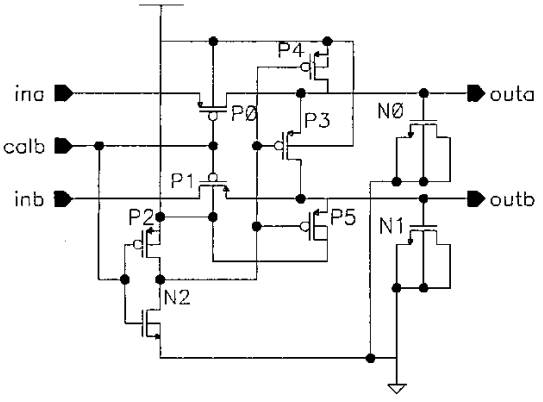

Figure 2. Transmission circuit

2.2. Flip-Flop Sensor and Data Detector

A new and simple flip-flop sensor has been developed, as shown in Figure 3(a). Circuit simulation verified its functionality and effectiveness. The flip-flop sensor is designed to be as simple as possible to avoid unnecessary mismatch and noise sources. When transistor P8 is turned on, the differential input signal inp/inn is amplified with pulldown transistors N1/N4 in series with calibration transistors N5/N6, working against pullup transistors P6/P7. The flip-flop nodes integrate the input signal until the cross-coupled pulldown transistors N2/N3 turn on, comparing the signal to the noise, and positive feedback results in a flip-flop decision. Simulations show that for a 1 μV input signal, the overall SNR of this design is at least 1/190, more than twice that of the previous design using a magnetic field based sensor [11].

The response of a stochastic sensor follows a Gaussian cumulative density function (CDF) around the metastable point [13][14][15][16]. This can be approximated as linear when the signal is much smaller than the noise, as shown in Figure 3(b). The probability of getting a "0" or "1" output from the flip-flop represents the equivalent magnitude of the analog input signal. The sign relative to 0.5 indicates whether the input is positive or negative (i.e. the direction of current flow). Since the slope of the CDF falls with rising noise amplitude, the "gain" of the stochastic sensor is inversely proportional to the noise. The noise has zero mean, so does not introduce an offset. The stochastic sensor achieves high sensitivity and high noise immunity through repetitive operation. Outputs of the stochastic sensor decisions, outn/outp, are fed into two 22-bits counters. With the slope of the CDF, the magnitude of the input can be deduced from the differences between these two 22-bits counters. In a production sensor only one counter is required.

The data detector works as a bridge to translate the flip-flop decision into proper calibration control signals and pass that to the calibration circuit. It produces non-overlapping pulse pairs pu1/pu2 and pd1/pd2, which pump up/down the calibration voltage through the calibration circuit. See Figure 3(c).

With a 2 to 1 multiplexer, the flip-flop decisions can be prevented from feeding into the counter during calibration. This permits calibration in the middle of a measurement cycle without disturbing the measured value. This enables "chopper" operation as discussed below.

2.3. Calibration Circuit

Although the flip-flop stochastic sensor achieves high gain, high resolution and noise immunity, it is extremely vulnerable to device mismatch, which is unavoidable in manufacturing. Due to the high gain, even a small mismatch will affect the resolution and accuracy. Therefore a calibration circuit is used to control the gate voltage of calibration pulldown transistors N5/N6 in the flip-flop stochastic sensor. Mismatch resulting from manufacturing or layout can be compensated for through a slight imbalance of the calibration transistor gate voltages.

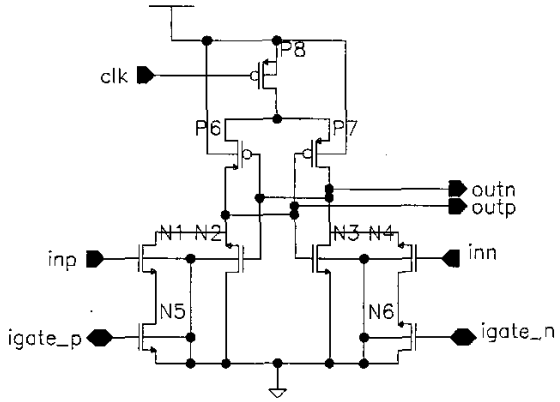

Figure 3(a). Flip-Flop Sensor

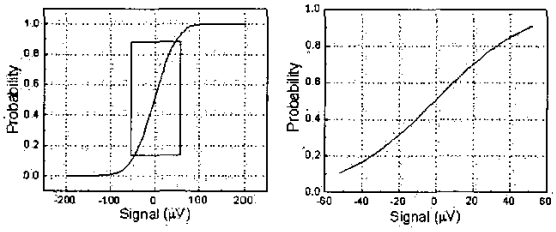

Figure 3(b). Conceptual transfer characteristic of the stochastic sensor. The rectangle region in (a) is shown in (b). This region can be approximated as linear when the signal is much smaller than the noise.

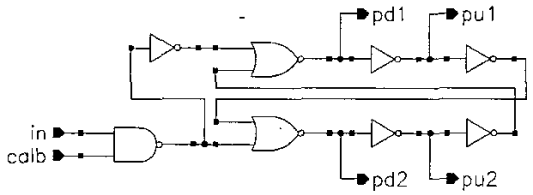

Figure 3(c). Data detector

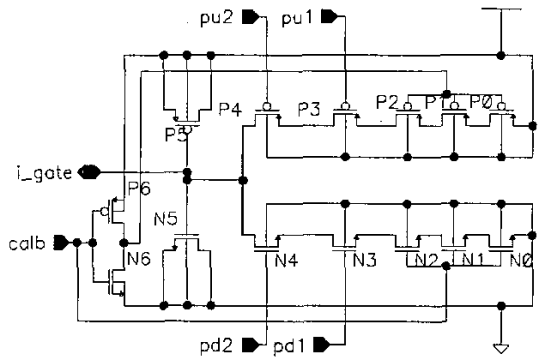

Figure 4. Calibration Circuit

The calibration circuit features high resolution, wide adjustment range and long holding time, as shown in Figure 4. Transistors P5/N5 act as the reservoir capacitor, with balanced gate oxide leakage paths. Transistors P3/P4 and N3/N4 form a charge pump with symmetrical pullup/pulldown paths. P3/P4 functions as pullups, controlled by the pull-up pulses pu1/pu2. To charge the reservoir capacitors, first P3 is pulsed to charge the P3/P4 parasitic junction capacitance and then P4 is pulsed to transfer the charge to P5/N5. Similarly, the discharge is through pulldown charge pump transistors N3/N4, which are pulsed by pd1/pd2. Stack transistors P0/P1/P2 and N0/N1/N2 are shut off after calibration is completed and significantly reduce leakage when holding the calibration voltage. The flip-flop stochastic sensor has 2 calibration circuits controlling the 2 calibration pulldown transistors independently. It is assumed that before calibration starts, the calibration node i_gate will leak to an intermediate voltage high enough to turn on pulldown transistors N5/N6 in Figure 3(a). This avoids the need for a startup circuit [11]. When mismatch occurs, the flip-flop stochastic sensor will mostly flip to one side. In this circumstance, the data detector generates such pulses that the calibration voltage on one side will ramp up while the other side ramps down to force the flip-flop back to the metastable state.

Since the area of the reservoir capacitors takes a considerable portion of the whole BICS area, the reservoir capacitors in 180 nm technology are sized for a calibration voltage drift of 1 μV/s at 25 °C. The size is a trade-off between BICS area and the desired holding time, since the larger the capacitor the longer the holding time. Over a 20 ms measurement interval, a 1 μV/s would produce an effective measurement error of about 10 nV or 1%. There are two primary challenges in the calibration circuit. The first is to achieve sufficient resolution to calibrate for any mismatch in the flip-flop. This is done with a suitable charge pump capacitance ratio, so that the minimum step in the flip-flop balance voltage is small compared to the 1 μV input signal. The second challenge is to make the drift during sensing small compared to the input signal. This is done by using high V_{TH} devices and stacking them [17]. The drift requirement of the calibration circuit is further reduced by using "digital chopping". In a standard chopper operation amplifier, the inputs are periodically shorted, and any observed output voltage difference stored on capacitors and then subtracted from the signal during sensing [18][19]. In our digital chopping approach, measurement is performed for a certain number of cycles, then recalibration is performed for a certain number of cycles, and then the process is repeated. During calibration the counters do not change, so the output value is not affected by the calibration cycles. By using shorter measurement and calibration periods, the drift requirements of the calibration circuit are relaxed. This permits the calibration circuit to be used in future leaky

technologies. Frequent recalibration also permits calibrating for temperature drifts and low-frequency noise.

2.4. Counter/Scan Chain

Since stochastic analysis is a sampling process, the number of samples N must be determined to achieve the desired measurement resolution. The required number of samples is described in section 3. We show that approximately 1 M samples are required. To provide extra capacity, a 22-bit counter/scan chain was implemented in the BICS system. A counter/scan chain cell is shown in Figure 5. In count mode (scanb is high) it forms a toggle flip-flop. In scan mode (scanb is low), pulldown transistors N9, N8/N5 and N6/N7 are shut off. Serial input T_1 is fed in to the master stage through transmission gate P4/N10 to inverter P0/N0. Weak inverter P2/N2 provides feedback to make the master static. Transmission gate P3/N1 and inverter P1/N1 form the dynamic slave latch to output T. Q1/Q1B and Q2/Q2B are the non-overlapping scan clocks. In count mode, N9 is on, Q1/Q1B is low, Q2/Q2B is high and transmission gate P4/N10 is off and transmission gate P3/N1 is on. The inputs T_1 and its inverse TB_1 control the pulldown paths N8/N5 and N6/N7. When N8/N5 is on, it pulls the input of inverter P0/N0 low, flipping the cell so that node B is high and outputs T low, and TB high. When N6/N7 is on, node A is high and node T high and TB low. Transistors N4 and N3 are used to store the previous state of A/B, and cause the cell to toggle on each input transition. The sequence of cells forms a ripple-carry counter. Since each bit flips at half the rate of the previous bit, the net active power dissipation of the counter is equivalent to two bits flipping every clock cycle. The counter/scan cell in is a simplified version of the one previously evaluated on test chips [11]. The design change, making the slave latch dynamic, improved the timing symmetry and margins of the toggle flip-flop. This also reduced the counter area by 20% and overall BICS transistor count by 16%. Circuit simulation shows that the counter operates at over 1 GHz in a 180 μm technology. Combined with the flip-flop SNR, overall IDDQ measurement time is as little as 1 ms (1 M clock cycles) for a high resolution measurement of a 1 μV signal, generated by 10 μA of IDDQ flowing in ten squares of 10 mΩ/□ wire. Even at typical scan clock rates, the measurement time of typical signals should be only 10-20 ms.

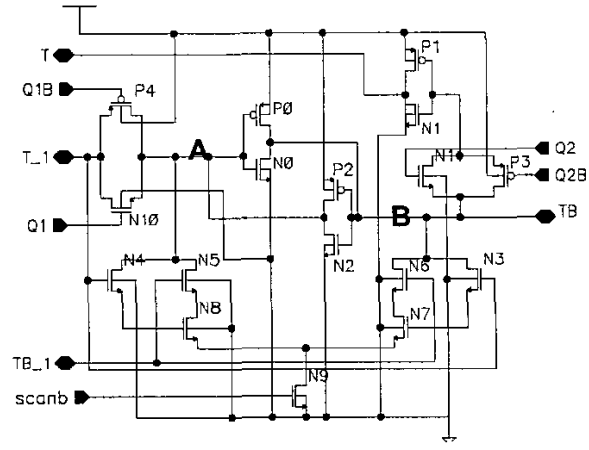

Figure 5. Counter/Scan Chain cell

2.5. IDDQ Sensor Operation

The operation of the proposed IDDQ sensor consists of four different operation modes: scan-in, calibration, measurement and scan-out. In the scan-in mode, the counter is reset by scanning in zeros serially. Similarly, the measurement results are scanned out using the counter/scan chain operating as a shift register. After scan-in zeros, the external calibration signal (CALB) will trigger the start as well as the end of the sensor's self-calibration. The normal measurement mode is initiated as soon as the calibration is performed. Measurement and calibration can be interleaved. Similarly, scanin and scanout can be overlapped. The tester interface can be simplified by having an on-chip controller generate the sequence of calibration and scan controls and Q1/Q2 clocks.

The total BICS area is 12,805 sq-μm in 180 nm CMOS, of which 80% is the conservatively-sized calibration reservoir capacitors. The sensor is expected to be at least four times faster for a given sensitivity, and is about four times smaller than the previous MAGFET-based sensor [11].

3. Experimental Results

In order to verify our design concept, a test chip has been fabricated using the MOSIS 1.5 μm AMI process. The chip measures 2.2 mm by 2.2 mm and is packaged in a 40-pin ceramic DIP. Chip layout is shown in Figure 6. The usable chip area is occupied by two full sensor systems as well as standalone system components, which enable us to test the functionality of each component of the sensor. The total number of transistors is 922 for the sensor system. If the production sensors use only one 22 bit counter then the number will be reduced to 534. The small white circles indicate the reservoir capacitors, larger reservoir capacitors (X16) are designated with the big circle in Figure 6. Several reservoir capacitor sizes are incorporated to

facilitate the study of calibration drift vs. capacitor size. The test fixture is based on a Xilinx FPGA Spartan system board D2E-DIO2. The FPGA was carefully programmed to generate test signals and store output results. An HP 1653B logic analyzer and an oscilloscope were also used to observe the output. A 40 MHz clock frequency was used for all measurement. This is the maximum clock rate of this test fixture. The chip was operated at 3 V to match the test fixture.

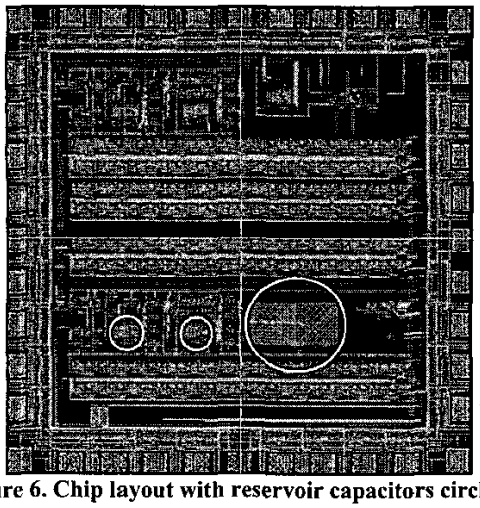

Figure 6. Chip layout with reservoir capacitors circled

The stochastic sensor transfer curve is shown in Figure 7. The Y-axis denotes the counter difference of the flip-flop decisions while the X-axis denotes the input value. One million repetitions are chosen for each measurement since this number will almost saturate the 22 bit counter. More repetitions would yield higher resolution, but takes longer test time. Longer test may cause test accuracy to suffer due to calibration drift. Note the value of each point in the figure is an average of 10 measurements. Calibration is always performed before each measurement. As shown in Figure 7, the stochastic behavior was observed. The gain of the sensor is approximately 800 counts/μV. Though calibration is done before each measurement, an offset of about 200 μV was observed, which is the result of a large calibration voltage step size as discussed below. From the transfer curve, an effective noise level of about 800 μV can be observed. This noise was found to be 4 times larger than our simulated noise level of 190 μV. Besides the internal noise, the external power supply was found to be the main source of noise. The supply noise is common mode in the calibration circuit and flip-flop, but is not completely cancelled, due to device mismatch.

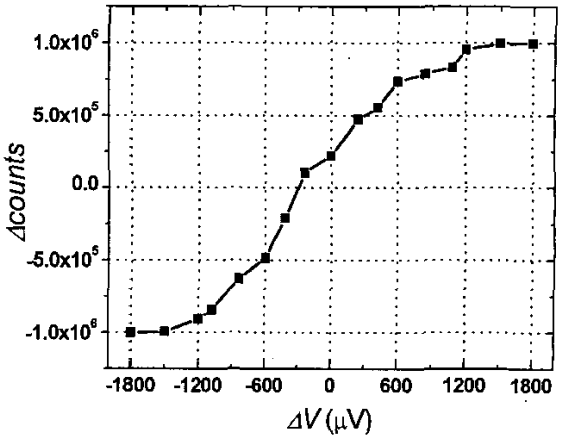

Figure 7. Measured stochastic sensor transfer curve

DeltaV(uV)	Average	σ
1800	1000000	0
1500	997933	2907
1200	953947	3224
1080	832050	4001
840	787326	3509
600	736727	2357
420	554643	3466
240	474376	2853
0	222930	3642
-240	100597	3198
-420	-208506	2487
-600	-485345	3414
-840	-627292	3795
-1080	-843434	5678
-1200	-908892	3760
-1500	-993616	4003
-1800	-1000000	0

Table 1. Counter average and standard deviation with respect to input voltage

The average counter difference and standard deviation with respect to input voltage is listed in Table 1. The predicted sampling variance is [20]:

$$\frac{pq}{N} \sim \frac{0.25}{N}$$

and the standard deviation equal to:

$$\sigma = [pq/N]^{\frac{1}{2}} \sim \frac{0.5}{\sqrt{N}}$$

where N is the number of repetitions while p and q are the probability for either side of the stochastic sensor to get a "1", which is close to 0.5 in our intended IDDQ test range. So we have the ±σ in counts equal to ±500 counts. The probability for a "one" decision is given by:

$$p \sim 0.5 \pm \frac{1}{\sqrt{2\pi}} \int_0^s \exp^{-1/2u^2} du$$

$$p \sim 0.5 \pm \frac{s}{\sqrt{2\pi}}$$

where s is the signal to noise ratio. So we have:

$$N \cdot p \sim N \cdot 0.5 \pm \frac{N \cdot s}{\sqrt{2\pi}}$$

In our measurement $\frac{N \cdot s}{\sqrt{2\pi}}$ is equal to 800 counts/μV vs. a σ of ±500 counts. So the 3σ sampling noise is ±1500/800 counts/μV, which is approximately 1.9 μV. This reflects a 19 μA resolution IDDQ for a 3σ confidence interval if 10 squares of 10 mΩ/□ metal are used for tapping the signal. The difference between two measurements has:

$$\Delta\mu = \mu_1 - \mu_2$$

$$\text{and } \sigma_\Delta = \sqrt{\sigma_1^2 - \sigma_2^2} = \sqrt{2}\sigma \sim 9\mu A$$

so we end up with about 60% confidence interval for a 10 μA IDDQ resolution. According to Table 1, the average standard deviation is 3076, which is about 6 times larger than the predicted sampling variance. The big calibration step size and the low frequency noise from the power supply are believed to cause this increased standard deviation.

Because of the older technology used and the chip area constraint, the sizing of the reservoir capacitor is limited and therefore the pumping ratio cannot achieve the targeted 1 μV step size suggested in the analysis section. For this design the ratio of pump capacitor to reservoir capacitor is close to 1 mV per step in simulation. This is about the same as the measured flip-flop mismatch of 1.2 mV. The measured average pump up and pump down step size was found to be 0.85 mV and 0.64 mV. The pumping step size is a variable and depends on the reservoir capacitor voltage in that it will approach 0 when the reservoir capacitor voltage is close to Vdd or Gnd. Although the step size is much bigger than the intended resolution, the combined work of pump up and pump down, or what we call the differential step, helps to calibrate the sensor in the metastable region. As illustrated in Figure 7, the transfer curve shows an offset of 200 μV, which is the result of the calibration differential step. This offset can easily be cancelled out by using the delta IDDQ technique. However, it poses an obstacle for our suggested digital chopping technique. This pumping step size problem can be greatly alleviated using state-of-the-art technology since the minimum pumping capacitance is drastically reduced as opposed to this older 1.5 μm technology.

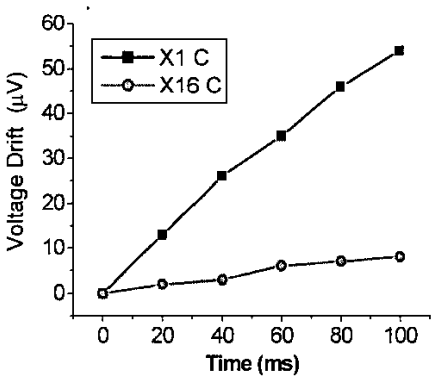

Figure 8. Calibration circuit drift rate

The measured drift rate of the calibration circuit is 12 μV per 20 ms, which is approximately an order of magnitude higher than the simulated results, as shown in Figure 8. This is due to elevated subthreshold leakage, which is caused by a weak "0" generated from the FPGA test fixture. The drift rate is found to be significantly improved by increasing the size of the reservoir capacitor. With the reservoir capacitor size enlarged by 16 times, the drift rate drops to less than 2 μV per 20 ms. Therefore a tradeoff must be made between the reservoir capacitor area and the desired drift rate.

4. Conclusions and Future Work

A practical Built-in Current Sensor (BICS) design is presented and components are described in details. This sensor system is able to monitor the IDDQ at a resolution level of 10 μA. This system can translate the current level into a digital signal, with scan chain readout. There is no system performance degradation for this sensor and its power dissipation is kept at a very low level. With the help of a self-calibration circuit, the sensor can maintain its accuracy and effectiveness. These concepts have been verified by a fabricated test chip.

Further work needs to be done to solve the stochastic sensor internal/external noise to achieve targeted sensitivity. The calibration drift concerns could potentially deteriorate due to elevated leakage in newer technology, although calibration step size becomes less of an issue.

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