Effectiveness of I-V Testing in Comparison to IDDq Tests

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Abstract

This paper will contrast the novel I-V test criteria with traditional and recent IDDq test methods. It compares their test effectiveness. We intend to show how I-V tests and IDDq tests fare in discriminating between "good" and "bad" dies and how test limits can be set empirically, especially for I-V testing. All results are based on data from an (internal) IBM experiment that was based on a large ASIC manufactured in a 0.18 µm-L_{eff} technology.

1. Introduction

Test of integrated circuits (ICs) has many purposes. The most common one is to screen defective ICs. Other purposes of IC test include learning about process or design sensitivities or interactions. The focus of this paper is to report how I-V testing can find outliers that are in addition to what is found and targeted by voltage tests or IDDq tests.

In an effort to help with product quality this paper investigates the effectiveness of some IDDq-based tests as found in the literature [4,5] as well as an IDDq-VDD curves-based test (or ***I-V test*** for short). The data is taken from an experiment run in IBM's Burlington, VT, fab in 1999-2000. The test vehicle was an ASIC design with 700,000 gates manufactured in a 0.25 µm CMOS technology with 0.18 µm-L_{eff}.

IDDq tests are used to ensure quality or to avoid burn-in rather than to ensure functionality of the IC [10]. The future merits of IDDq-based tests have been challenged due to the rising IDDq values and more importantly due to the increasing variations of IDDq values [6,9]. We will very briefly summarize how other authors have tackled this problem and then focus on the use of I-V testing to alleviate these obstacles, as we believe that despite these obstacles IDDq measurements afford a great source of information about the condition of the circuit.

Section 2 will recapitulate the ideas of some IDDq-based tests whereas Section 3 introduces the new ideas used for IDDq-VDD curves-based testing. Section 4 summarizes the data that was collected during the experiment and Section 5 uses this data to evaluate test effectiveness of the different tests described in Sections 2 and 3. This report ends with an outline of future work and our conclusions.

2. IDDq-based tests

2.1. Background of IDDq testing

The simple idea behind IDDq based tests is that a defect-free fully complementary CMOS circuit has no static current paths. In a circuit with a defect, however, a direct current path exists if the right excitation pattern is applied. (Shorts between power rails, however, can cause high static power consumption independent of the pattern).

Figure 1 explains this idea with an example. If there is a circuit deformation leading to a resistive short between two signal nodes (*here*: *x* and *y*), extra current will flow through the pull-up network of one driver (*here*: PMOS transistor in the NAND gate), the defect itself (*here*: R_{defect}), and the pull-down network of the other driver (*here*: NMOS transistor of the inverter)—provided that the input vector leads to (at least one) PMOS and the NMOS transistor being on.

IDDq testing works by applying the "right" pattern and measuring the extra current flowing through current paths that would not exist without a defect. The following methods differ in how the IDDq measurements are used to discriminate between defect-free and defective dies. The brief descriptions cannot do full justice to these methods and the reader is referred to the original publications for implementation details [4-7].

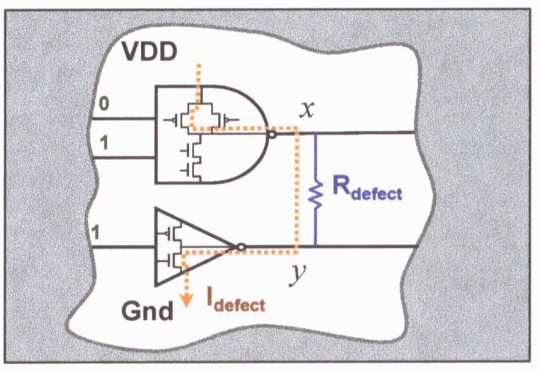

Figure 1. Example for a direct current path.

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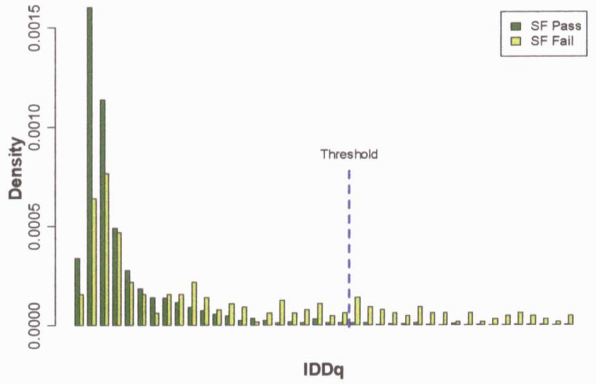

Figure 2. Histogram of IDDq for first pattern separated by voltage test results.

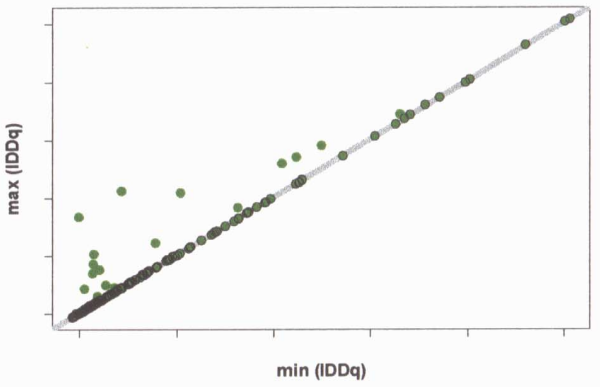

Figure 3. Scatterplot of maximum vs. minimum IDDq measurement for 4 test patterns (learning sample).

2.2. Traditional IDDq test method

Figure 2 shows the histograms of two IDDq distributions combined into one plot. The values along the x-axis have been omitted to protect the proprietary data, but note that this axis covers almost an entire order of magnitude of current. The population of "good" dies (labeled '***SF pass***'), which pass voltage and delay tests, has a distribution with a clear center on the left. This is in contrast to the population of the "bad" dies (labeled '***SF fail***'), which failed at least one voltage test pattern. This distribution has a much wider and heavier tail towards higher IDDq.

The *traditional IDDq* test then uses a threshold to cut off outliers whose IDDq value is so high that the extra IDDq can be assumed to be caused by a defect. Some dies that pass voltage test but whose IDDq value is above the threshold are eliminated. But note that only few of the '*SF fail*' dies fail this test. For some defective dies, the defect was not excited with the first IDDq test pattern. So often more test patterns are applied and the maximum is used in the test decision. As Section 5 will show, taking more test patterns does aid, although not much, in separating the two distributions more clearly.

2.3. Delta IDDq

Since using a single threshold has become unwieldy due to the large variations in IDDq and the increasing overlap of the distribution of defect-free and defective dies, another method to use IDDq measurements, *Delta IDDq*, has been proposed [4]. It uses for the test decision the difference between two consecutive measurements. This is done to eliminate the large die-to-die variations in quiescent current and has the potential to focus the testing on the additional defect current.

2.4. Current Ratios

Another method, which was proposed in [5], uses current ratios. The first observation from the data is that at least for good dies there is a strong correlation evident between the highest (*Max*) and lowest (*Min*) IDDq measurement from several test patterns on one die. Thus a relationship between these two measurements has been suggested:

$$Max = Slope \bullet Min + Intercept .$$

Slope and *Intercept* can be found using linear regression. Points that fall away from the gray line shown in Figure 3 by more than $3 \cdot \sigma_{residuals}$ are considered outliers. These points are iteratively removed for the learning sample until no more outlier points exist.

This motivates two test limits as follows. The IDDq is measured with a previously selected test vector applied. (This pattern is expected to produce the lowest IDDq value, see [5] for this ranking.) The theoretical limit for the highest IDDq is calculated from this measurement and subsequent measurements are compared against this limit:

$$T_{upper} = Slope \bullet Min_{measured} + Intercept + Outlier$$

If any measurement is higher than this upper limit, additional current flows and the die is rejected. If any measurement is lower than the lower limit, additional current was flowing during the first measurement and the die is rejected. This lower limit is set as:

$$T_{lower} = Min_{measured} - Outlier$$

The *Outlier* margin is $3 \bullet \sigma_{residuals}$ in both cases.

3. IDDq-VDD based testing

Since there were promising results from a previous experiment, IDDq-VDD measurements were added in the test flow during wafer-level and packaged-die tests for all dies in this experiment. This section describes what those extra

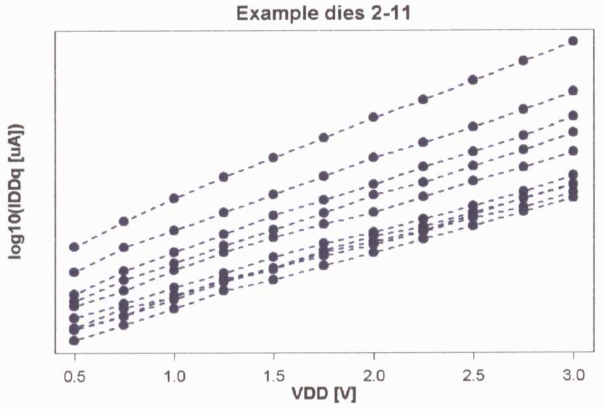

Figure 4. Example I-V curves for good dies.

measurements are and how extra information can be derived. Methods based on multiple measurements of IDDq at different VDD values have been previously suggested, *e.g.* [1, 3].

3.1. Basic idea

While it is possible to extend IDDq tests by using more test patterns, there is another dimension worth exploring: the static power supply current (IDDq) can be measured at different power supply voltages (VDD values). This opens up more possibilities to sieve out or through defective dies.

First, the shape of the curve, *i.e.* the relationship between IDDq and VDD, is expected to vary little for good dies. Figure 4 gives graphical support for this assumption. The model fit values described in Section 3.2 give numeric support. For defective parts, the shape may vary, however, and may even vary significantly. Second, the current flowing through the defect or other connected logic may not vary as expected from the "normal" IDDq-VDD relationship. In other words the mix of additional (defect) current may change with VDD. Third, different leakage mechanisms may dominate at different power supply voltages. Thus also the leakage split among the different mechanisms varies with VDD.

In this experiment, the power supply voltage was always ramped down. This has the advantage that one can use the scan chains to control the circuit state by applying a test pattern.

3.2. Data analysis (compaction)

Given that there are between seven and 15 measurements on thousands of dies and a plethora of shapes defining the I-V curves for bad dies, a strategy had to be devised to handle this amount of data with the purpose of comparing properties among dies, gaining insight into main distributions, and developing outlier criteria.

A model that has worked very well with the industrial data and the simulation results is simply:

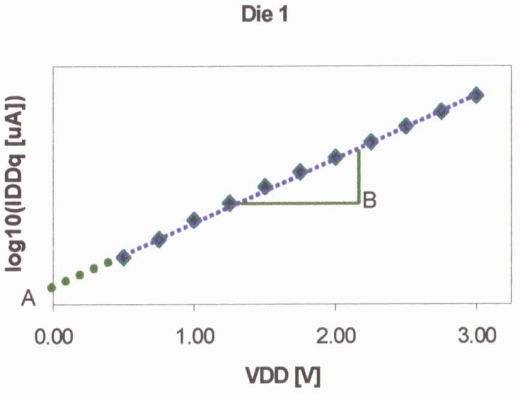

Figure 5. Example IDDq-VDD model and model parameters.

$$\log_{10}(IDDq) = A + B \bullet VDD\,.$$

Thus a linear regression of $\log_{10}(IDDq)$ vs. VDD yields two model parameters (A and B in this equation) as well as R^2, which measures the model fit. Figure 5 shows for data from one die the actual measurement points and the fitted curve, which is a straight line in this simple model.

Figure 6 contains the histogram of R^2 values for dies that pass voltage tests and, separated, for dies that fail any voltage test. The vast majority (99%) of "good" dies have an excellent model fit ($R^2 > 0.99$).

3.3. Test criteria

For our purposes, a die is considered an outlier under two conditions: (1) the model parameters fall outside an acceptability interval defined by the good dies or (2) the model fit is poor.

The test criterion presented in this section works with the two model parameters, A and B, that were introduced above. The quality of the model fit (R^2) could (and should) also be used in establishing whether a die is an outlier. The criterion

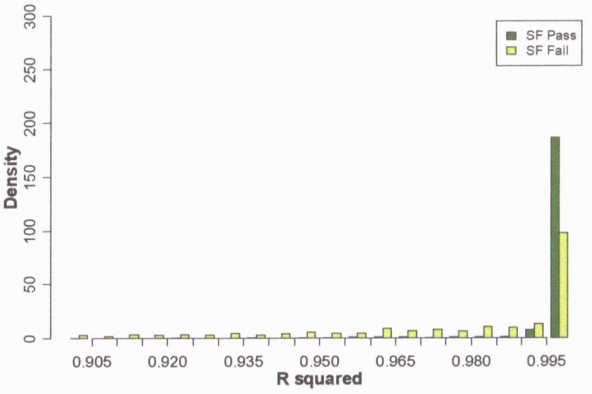

Figure 6. Histogram of R2 values.

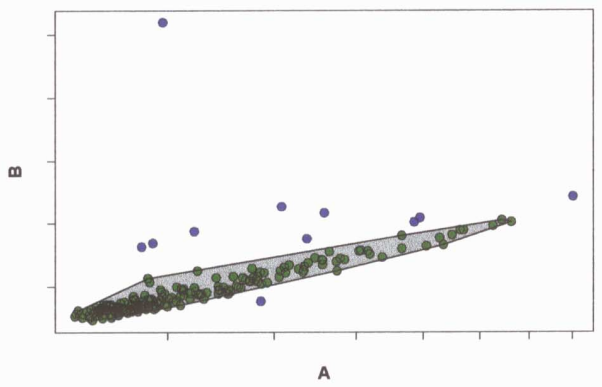

Figure 7. Scatterplot of model parameters from I-V test on first pattern.

does not (yet) cover test pattern-to-pattern variations.

When the model parameters A and B are plotted for good dies, they cluster (see Figure 7). However, a few points from outliers fall outside the region defined by the points from normal dies. The goal is then to find this region of good dies, which has been inserted in Figure 7. Our test criterion is whether the point from the model parameters falls within this region. If the IDDq(VDD) curve was measured for more than one pattern, then a die passes this test if points for the I-V models fall within the acceptance region for every test pattern.

A greedy heuristic, described in Figure 8, has been devised to determine an acceptance region. An alternative approach could be based on principal component analysis that would work with $3 \bullet \sigma$ rectangles or $3 \bullet \sigma$ ellipsoids around the region where the points from good dies cluster.

Note that this covers dies that have elevated background current as the intercept parameter would increase.

4. Summary of tester data

The data set contained the IDDq measurements for 52 voltage test patterns, results from voltage and parametric tests for all dies in one wafer lot. Dies that failed on the tester for tests of connectivity or opens were removed as well as dies that had seen special process treatment in a wafer split.

The population of dies that passed voltage tests was split into two: one set used for learning (11%) and one set used for validation (89%). The population of dies that failed any voltage test was always used only for validation. The results shown in the next section were based on *wafer-level* measurements.

5. Test effectiveness

This section shows results for each individual test method presented in Sections 2 and 3. Results are always split for the two validation data sets explained in Section 4. Table 1

Preparation step: Normalize the two model parameters (using a robust estimation of the center and the widths of the parameter distribution)

Initial step: Include all dies in the acceptance region by finding the convex hull over all points from dies in the learning sample.

Incremental step: Examine all points on the convex hull and drop that point which reduces the area inside the hull the most. Find the new convex hull of the remaining data points.

Last step: Quit when area reduction is below user-set limit.

Figure 8. Algorithm to find central region with greedy heuristic.

summarizes the percentage of dies that pass or fail the IDDq test named in column 1 separately for the two validation test sets. The threshold/limits used by any method were set by inspecting the learning sample.

Traditional IDDq: After removing severe outliers a value $3 \bullet \sigma$ above the mean of the distribution was used. For either number of test patterns, 3% of the dies that passed voltage test had maximum IDDq measurements above this threshold. About half of the dies that failed voltage test also failed this test.

Delta IDDq: Why this method only fails 40% of the dies that already fail voltage tests while adding little for dies that pass voltage tests is not yet clear. But the results for 52 test

Table 1. Test results for the test methods presented.

Test Method	*SF Pass*		*SF Fail*	
	Pass	**Fail**	**Pass**	**Fail**
Traditional (4 test patterns)	96.8%	3.2%	51.1%	49.9%
Traditional (52 test patterns)	96.8%	3.2%	46.7%	53.3%
Delta IDDq (4 test patterns)	97.6%	2.4%	61.7%	38.3%
Delta IDDq (52 test patterns)	96.3%	2.7%	40.5%	59.5%
Current Ratios (4 test patterns)	92.9%	7.1%	34.3%	65.7%
Current Ratios (52 test patterns)	88.5%	11.5%	28.1%	71.9%
I-V Testing (1 test pattern, 11 measurements)	88.6%	11.4%	28.9%	71.1%
I-V Testing (3 test patterns, 11 measurements ea.)	88.6%	11.4%	19.0%	81.0%

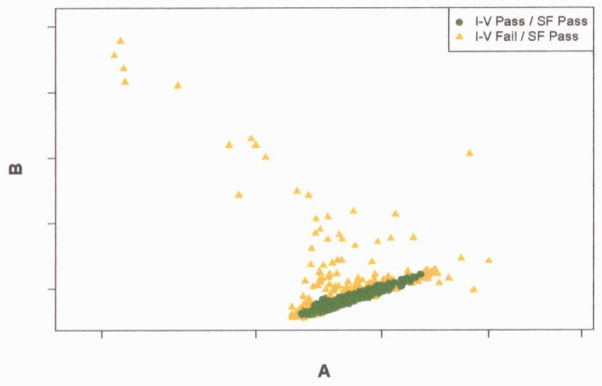

Figure 9. IV-Test results for dies passing voltage tests.

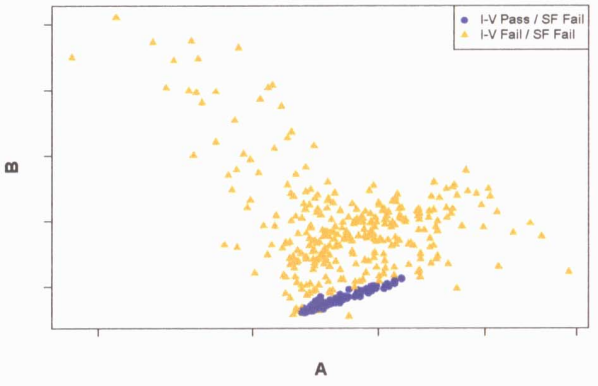

Figure 10. IV-Test results for dies that fail voltage tests.

patterns show the improvements this method has to offer.

Current Ratios: The thresholds T_{upper} and T_{lower} are set for each die individually by calculating them from the IDDq measurement on the lowest-ranked vector. The values of *Slope* and *Intercept* were determined using the learning sample.

I-V Tests: The results are based on the acceptance region shown before in Figure 7. Figure 9 shows the results from dies in the validation set that pass voltage test and supports the claim that almost all dies cluster in one contiguous region. It must be observed that dies are (currently) rejected at the edges of that region. Improvements to this method are being made to increase the cover of the nominal cluster enough to include the dies at the edges (which are marginal from the perspective of geometry, but not reliability).

Figure 10 shows the results from dies in the validation set that fail voltage test. It offers a striking contrast to the previous figure in that the spread of the model parameters is much larger. For most dies that fall outside the acceptance region, the model fit is also low. Figure 11 shows some I-V curves of dies that were uniquely rejected by I-V tests.

While more dies that pass voltage test fail I-V test compared to the IDDq test methods, which is a yield loss that can be amended by better test criteria, this test method also fails the highest percentage of dies that fail voltage test. This is interesting in two ways: The more *SF fail* dies that the method fails, the lower the number of false rejects of *SF pass* dies may be. And more importantly, at reduced voltages some defects become visible that are missed by the other IDDq tests [3].

Figure 12 shows two diagrams that allow to judge what each of the "enhanced" IDDq and the I-V Test method uniquely detect or reject. The left hand side of Figure 12 contains the data for dies that pass all voltage tests as well as the traditional IDDq test, which is defined in Section 2.2. I-V tests pass 24 of the dies that both, IDDq Delta and IDDq ratios reject. The right hand side contains the data for dies that fail any voltage test as well as the traditional IDDq tests. I-V tests fail 20 dies that neither IDDq Delta nor IDDq current ratios detect.

Summarizing Table 1 graphically, Figure 13 shows two data points for each test method: "Pass/Pass" is the percentage of dies that pass voltage tests and also pass the particular IDDq test. "Fail/Fail" is the percentage of dies that fail any voltage tests and also fail the particular IDDq test.

The comparison of the test methods is done implicitly with respect to the results of voltage test. This may not be optimal but it should allow a comparison of what each test method additionally accepts or rejects. Coverage of less than 100% for any IDDq test method for passing dies indicates that the particular test rejected some of these dies as defective. A coverage of less than 100% for any IDDq test method for failing dies is to be expected as many more test patterns are exercised for voltage tests than are for IDDq tests and for some dies the defect is never excited and hence not observable in IDDq measurements.

A detailed analysis of the dies that fail I-V tests is required to understand how many of the dies, which fail I-V

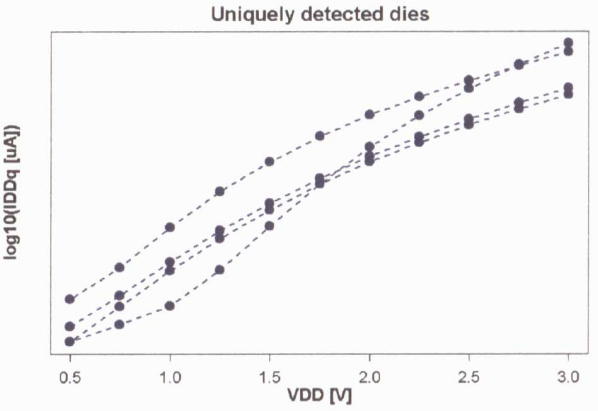

Figure 11. Example dies that failed only IV-Tests.

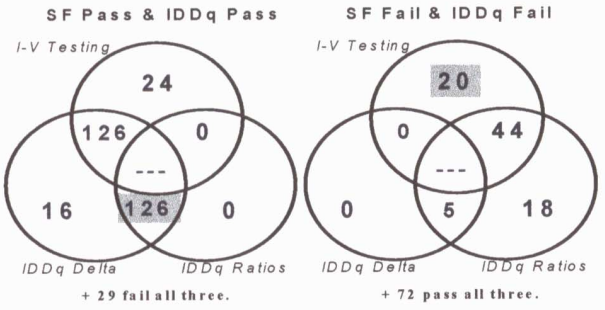

Figure 12. Venn diagrams with numbers of unique accepts and rejects of IDDq Delta, Current Ratios, and IV-Tests.

test, are actually defective. Compared to traditional IDDq tests using 52 test patterns, 8% more dies fail (just one more die than with current ratios). Using just one pattern, I-V Tests deliver better coverage for failing dies than most other IDDq test. Using three patterns (for a total of 33 measurements) I-V tests provide the best coverage of failing dies. Whether this coverage indicates that all the good dies rejected by this method are actually defective is under investigation.

6. Conclusions

The original intent behind this paper was to compare several variations of IDDq tests and IDDq-VDD testing. Section 5 showed that I-V tests have the capability to perform quite well to discriminate outliers from good dies. I-V tests do incur a higher cost on the tester compared to hundreds of voltage test patterns that could be run in the same time, but for some products they may be worth applying to improve product quality.

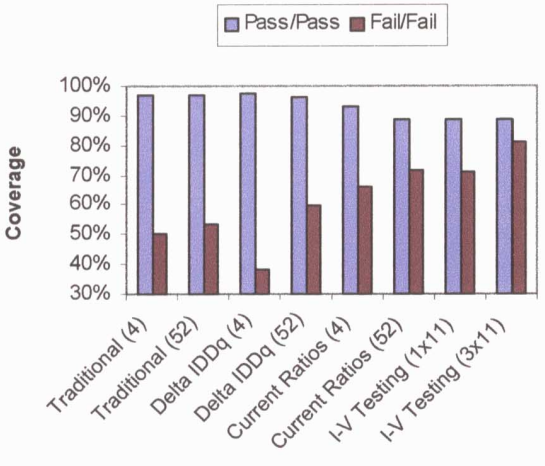

Figure 13. Comparison of coverage of passing and failing dies by IDDq methods. The number of test measurements used is in parentheses after a method's name.

There are limits as to what IDDq tests will be able to deliver in the future. With rising background currents and their increasing variance, IDDq tests face hard challenges. Nevertheless, the power supply current does afford an insight into the analog behavior of a die and an IDDq-VDD approach could help in the future to (1) find parametric outliers, (2) examine process windows, and (3) characterize physical attributes of defects. Similarly, the simple model presented in Section 3.2 will have to be reviewed and revised for future technologies. Rather than to improve test methods *per se*, we intend to exploit these capabilities in the future to improve our insight into process deviations and defect characteristics.

Acknowledgements

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