Testing of Integrated Circuits

J. Christiansen
CERN - EP/MIC
Jorgen.Christiansen@cern.ch

Cost of finding failing chip

LEVEL	FAILURE MECHANISM	PRICE
Specification	Functionality, Performance Testability, reliability Interoperability	1$
Design	——— 〃 ———	1000$ 100 $
Prototype	Verification, Qualification, Production margins	100.000$ GOLD
Wafer	Yield, speed, noise, gain	1$
Chip	Cutting, bonding	10$
(MCM) Module	Soldering, ESD	100$ 100 $
(Sub) System	Cables, connectors	1000$ 100 $
At customer	Reliability of components, vibrations, corrosion, radiation, high voltage	10.000$ GOLD

Design verification testing

(price per design)

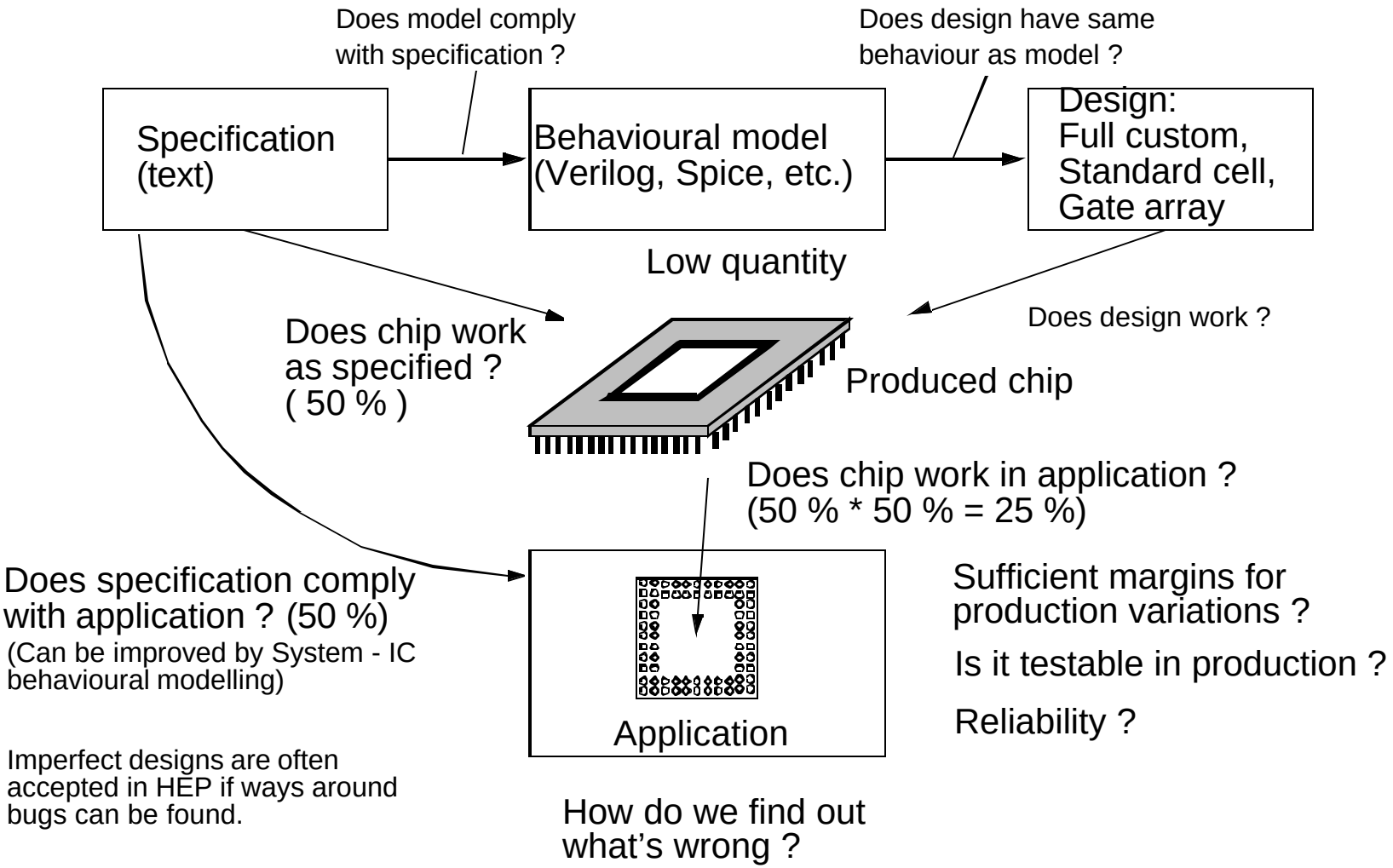
100K$ - ? $
(if not sufficient design verification performed)

Production testing

(price per chip)

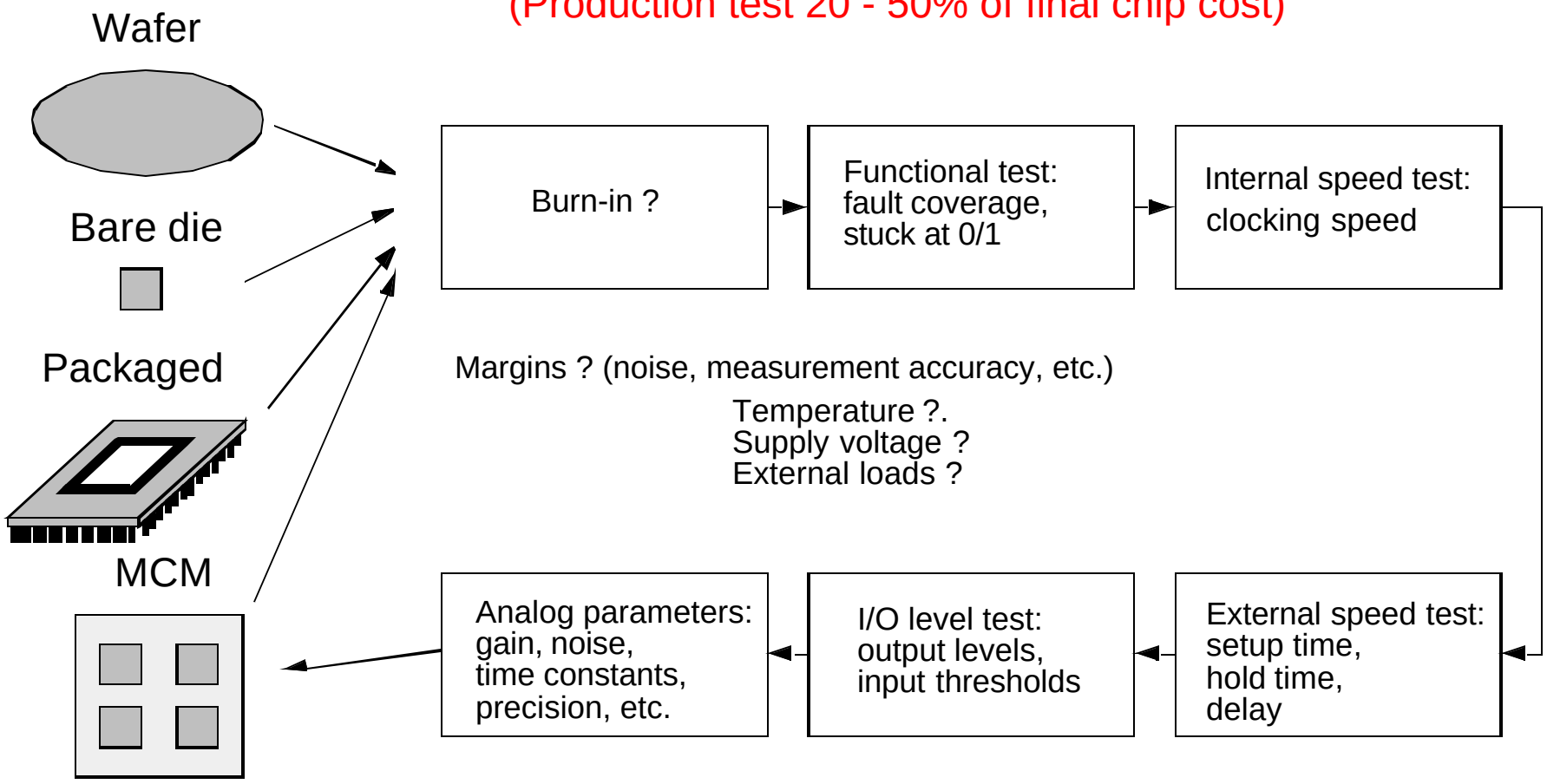
Design verification testing

(10- 50% of total development costs)



Production testing

(Production test pattern development 5 - 25 % of development costs)
(Production test 20 - 50% of final chip cost)

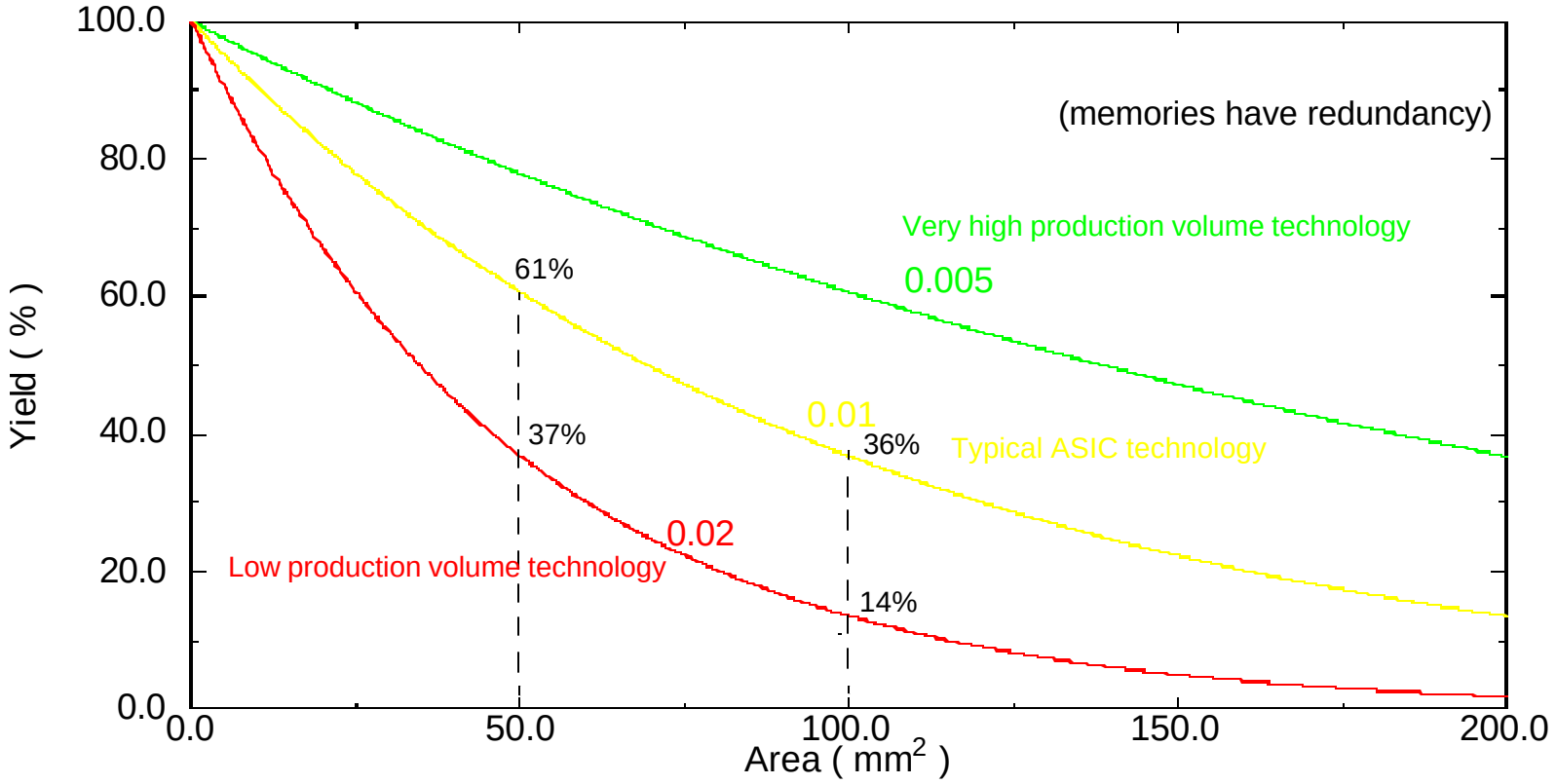


Monitoring of radiation resistance (destructive test)

Production yield

Yield is calculated from defects per mm^2 (= exp(- A * D))

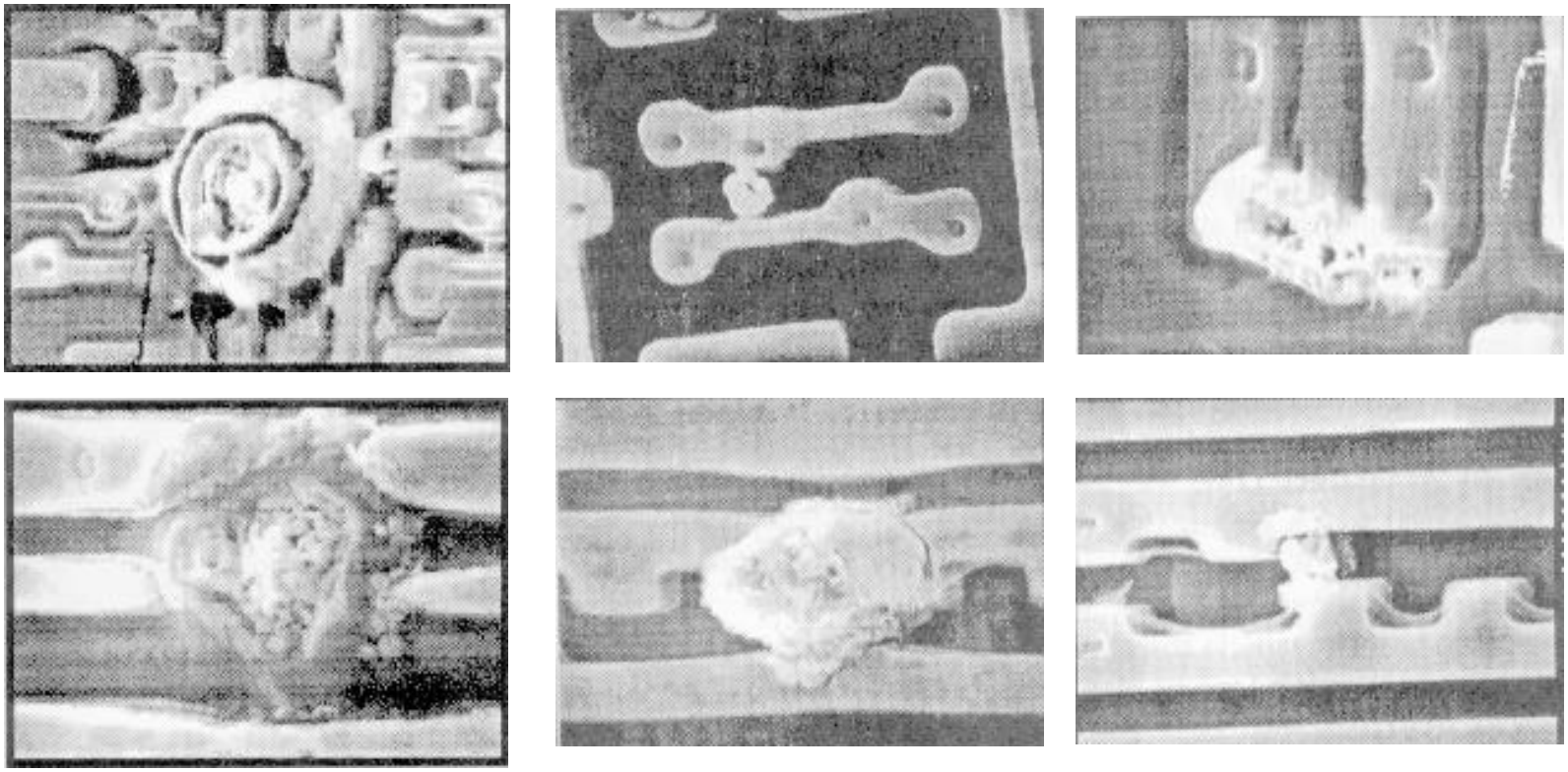
Typical defect density is of the order of 0.005 - 0.02 defects/mm^2



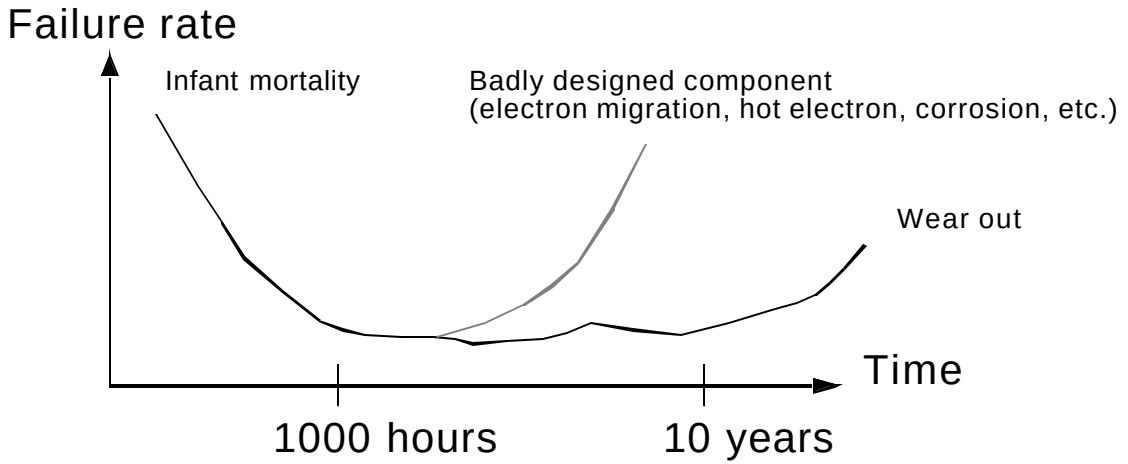
Price of 100 mm^2 chip compared to 50 mm^2 chip: 100 mm^2/50 mm^2 x 0.61/0.37 = 3.4 (D=0.01)

100 mm^2/50 mm^2 x 0.36/0.14 = **5.3** (D= 0.02)

Typical IC faults



Reliability of integrated circuits



Failing parts within first 1000 hours: 1 - 5 %

Burn-in testing : Heating up chips to 125 deg. accelerates 1000 hours period to approx. 24 hours.

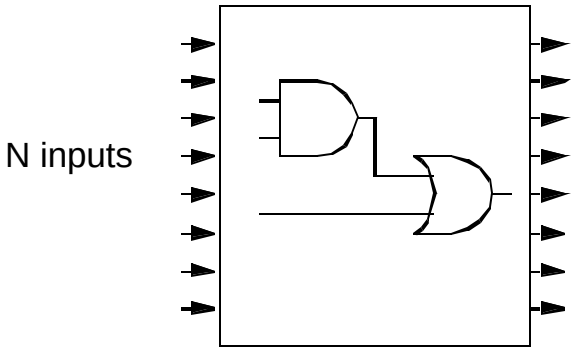
Static: power supply connected.
Dynamic: Power + stimulation patterns.
Functional test: Power + stimulation patterns + test.

Temperature cycling: Continuous temperature cycling of chips to provoke temperature gradient induced faults.
(Non matching thermal expansion coefficients).

Electrical stress: Operation at elevated supply voltage

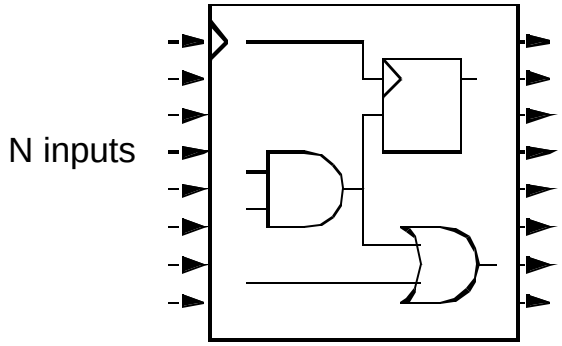
What to test

Combinatorial



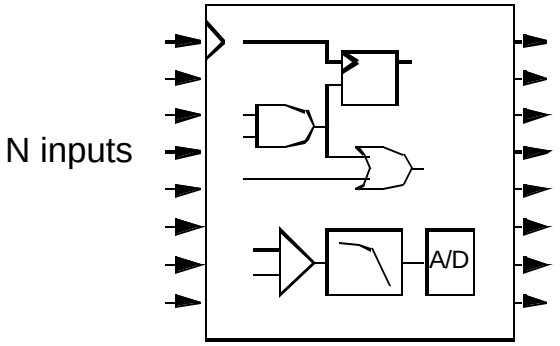
Exhaustive test vectors: 2^N

Sequential



Exhaustive test vectors: $2^{(N+M)}$

Mixed analog/digital



Exhaustive test vectors: $2^{(N+M)}$
plus analog parameters

100 Mhz tester:
N=32 ; test time = 40 seconds.
N=64 ; test time = 6.000 years

Knowledge about topology of circuit must be used to reduce number of test vectors so they can be generated by tester (tester memory: 10K - 10M).

Analog and digital stimuli must be generated from a tightly synchronised system.

Basic testing terms

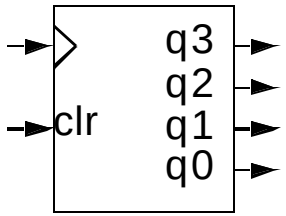
CONTROLABILITY: The ease of controlling the state of a node in the circuit.

OBSERVABILITY: The ease of observing the state of a node in the circuit

Example: 4 bit counter with clear

Control of q3:

Set low: perform clear = 1 vector



Set high : perform clear + count to 1000B = 9 vectors

Testing a node in a circuit

A: Apply sequence of test vectors to circuit which sets node to demanded state.

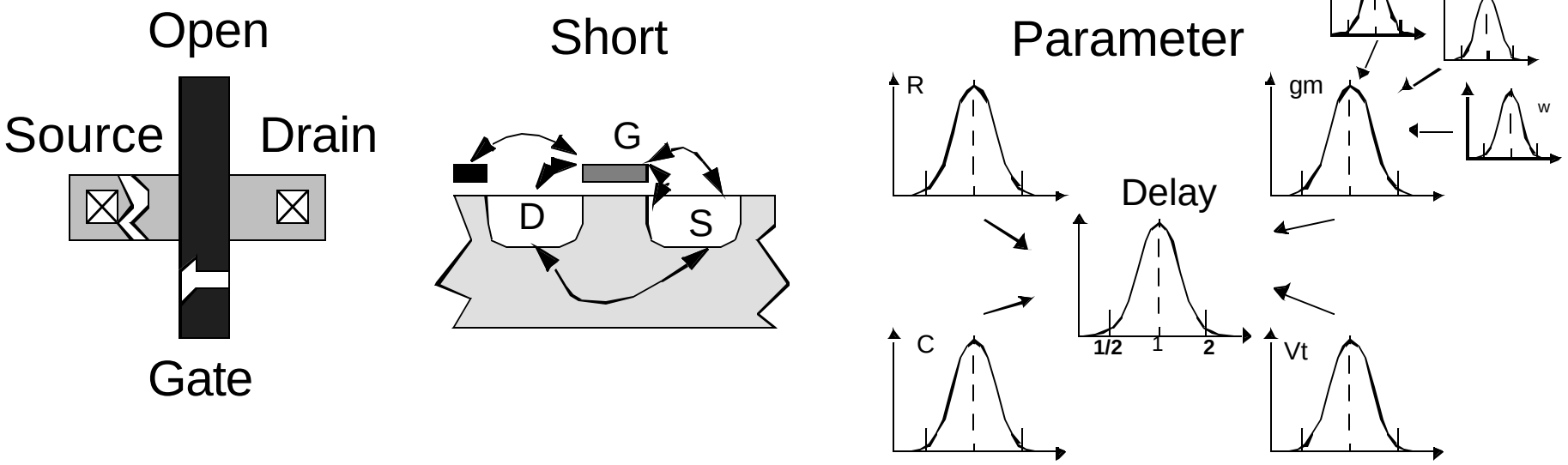
B: Apply sequence of test vectors to circuit which enables state of node to be observed.

C: The observing test vector sequence must not change state of node.

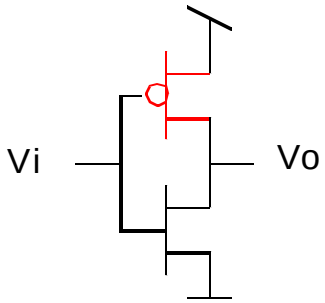
Fault models

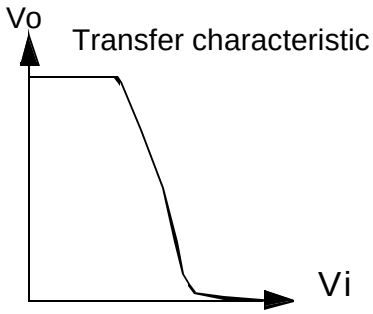
Fault types: Functional.
Timing.

Abstraction level: Transistor. (layout)
Gate. (netlist)
Macro (functional blocks).

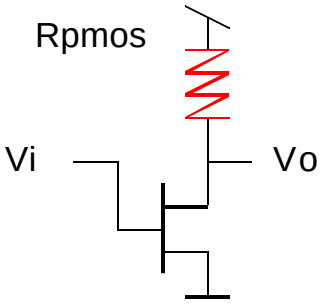


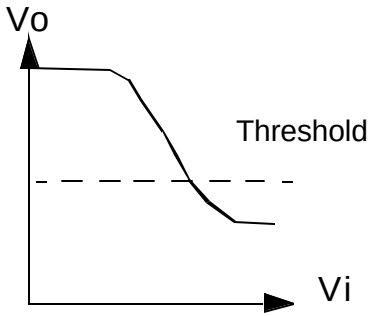
Problematic faults at transistor level



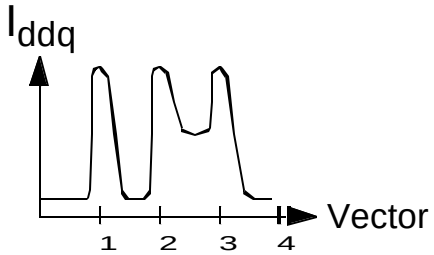


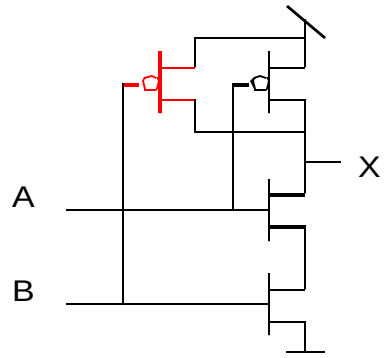
PMOS stuck on





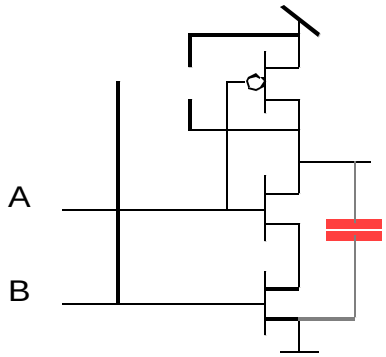
CMOS logic may become NMOS logic.





A	B	X
0	0	1
0	1	1
1	1	0
1	0	1

PMOS stuck open

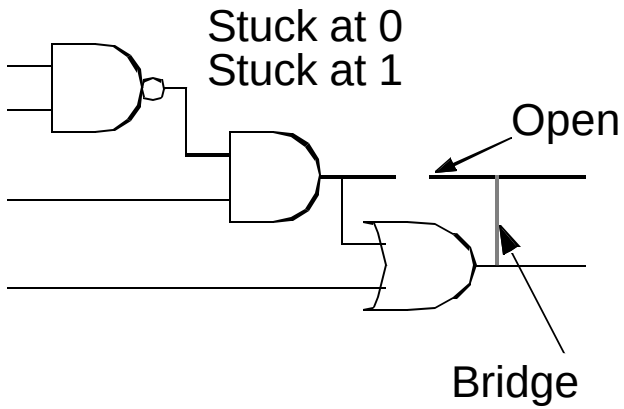


A	B	X
0	0	1
1	0	1
1	1	0
0	1	1

A	B	X
0	0	1
0	1	1
1	1	0
1	0	0

Combinatorial logic may become sequential

Gate level (stuck at 0/1model)

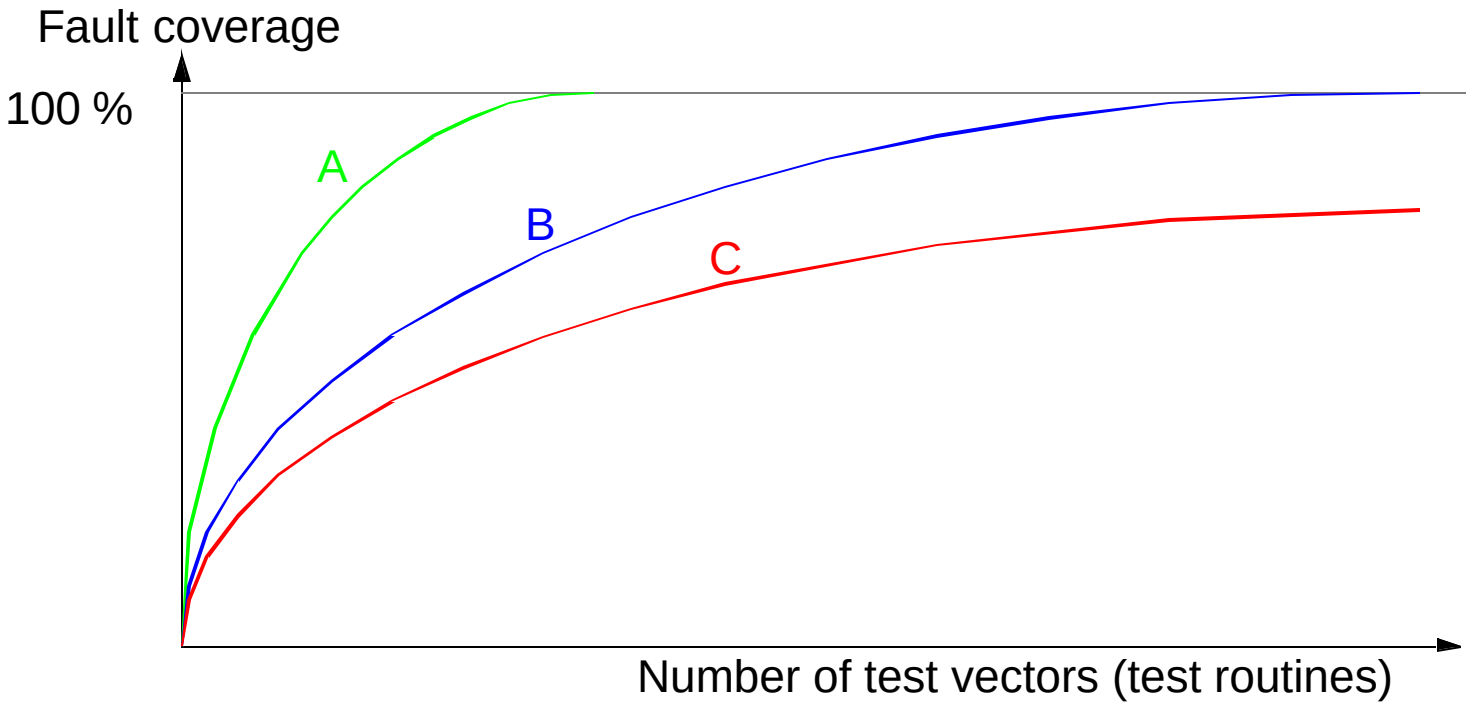


The gate level stuck at 0/1 is the dominantly used fault model for VLSI circuits, because of its simplicity.

Fault coverage calculated by fault simulation are always calculated using the stuck at 0/1 model. Other more complicated fault models are to compute intensive for VLSI designs.

$$\text{Fault coverage} = \frac{\text{Number of faults detected by test pattern}}{\text{Total number of possible stuck at faults in circuit}}$$

Testability



A: Design made with testability in mind. (~1 test vector per gate)

B: Design made without testability in mind but good fault coverage obtained by large effort in making test vectors.

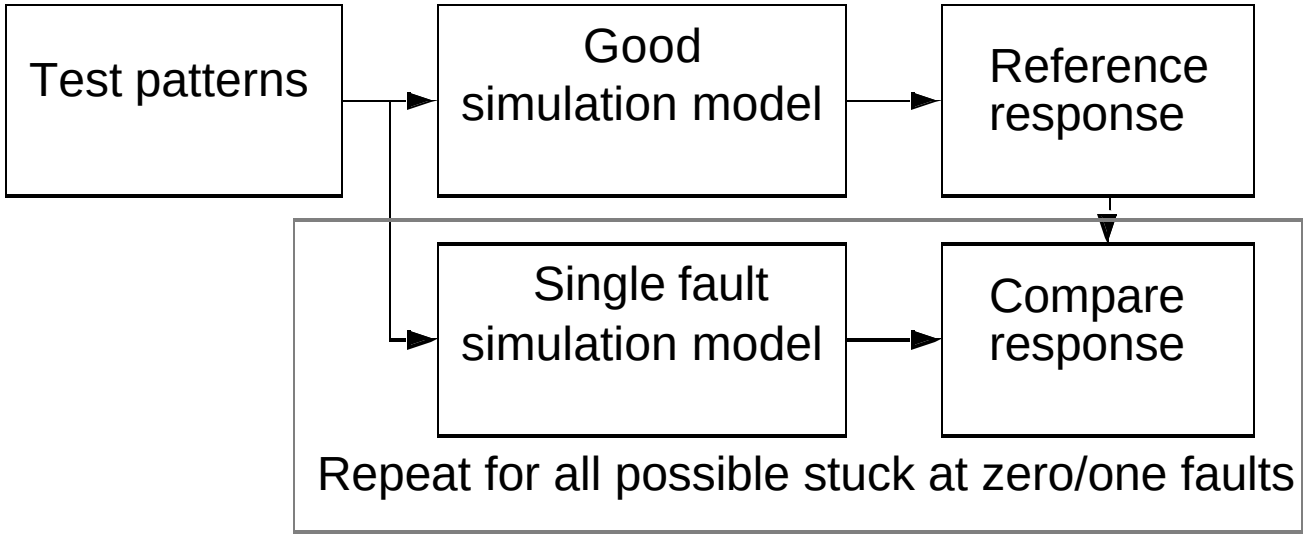
C: Design very difficult to test even using large effort in test vector generation.

Generation of test patterns

- Test vectors made by test engineer based on functional description and schematics. Proprietary test vector languages used to drive tester. (over the wall)
- Test vectors made by design engineer on CAE system. Subset of test patterns may be taken from design verification simulations.
- Generated by Automatic Test Pattern Generators (ATPG). Requires internal scan path
- Pseudo random generated test patterns.
- Fault simulation calculates fault coverage.

Fault simulation

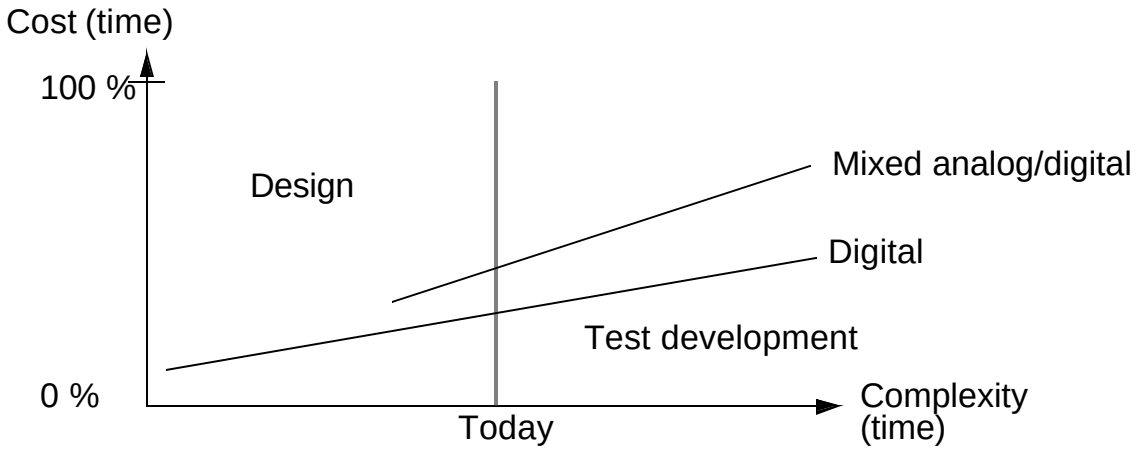
Fault coverage found by fault simulations



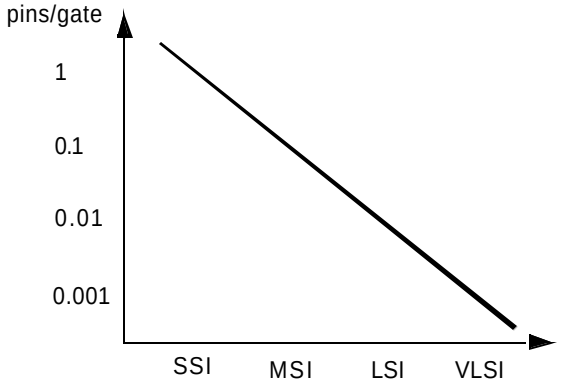
Requires long simulation times !.

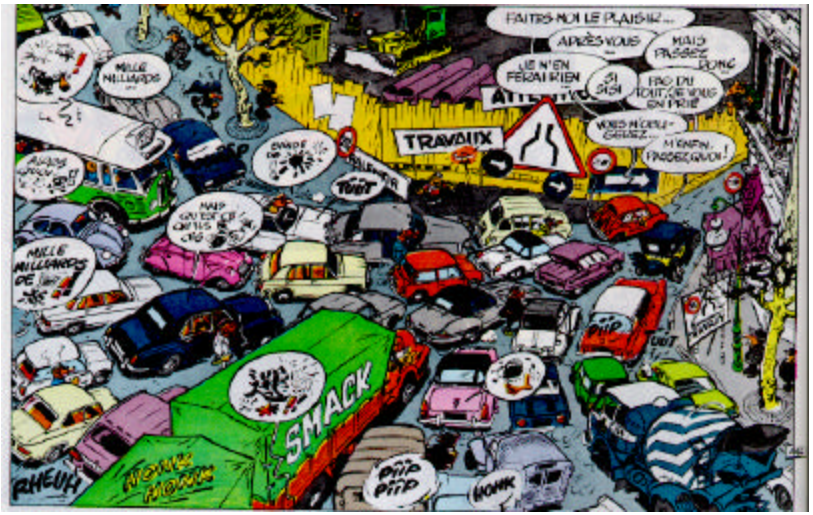
Toggle test (counts how many times each node has changed) can be used to get a first impression of fault coverage.

Test development with increased complexity



Testability is decreasing drastically with increased integration level



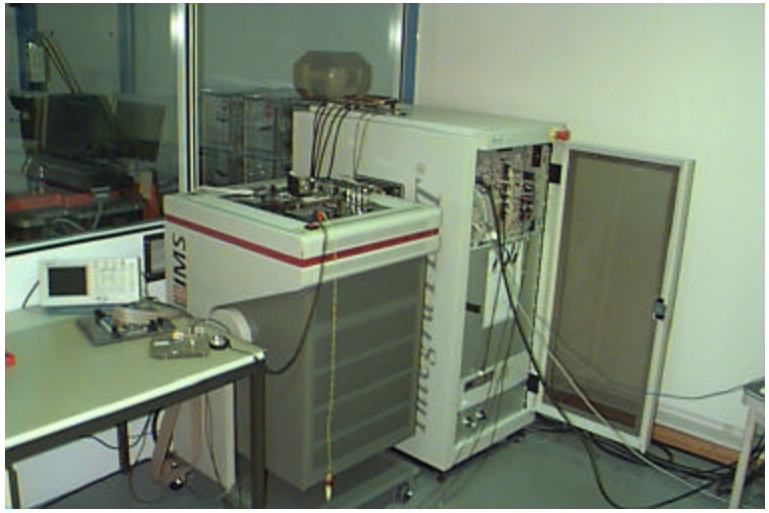


IC testers

High speed high pin count VLSI testers are very expensive and complicated machines. (500 k$ - 10 M$).

Vector speed: 100 - 1000MHz,
Vector depth: 32k - 1G
Time resolution: 100ps - 10ps
Pin count: 100 - 1024

"Cheap" = 500k$

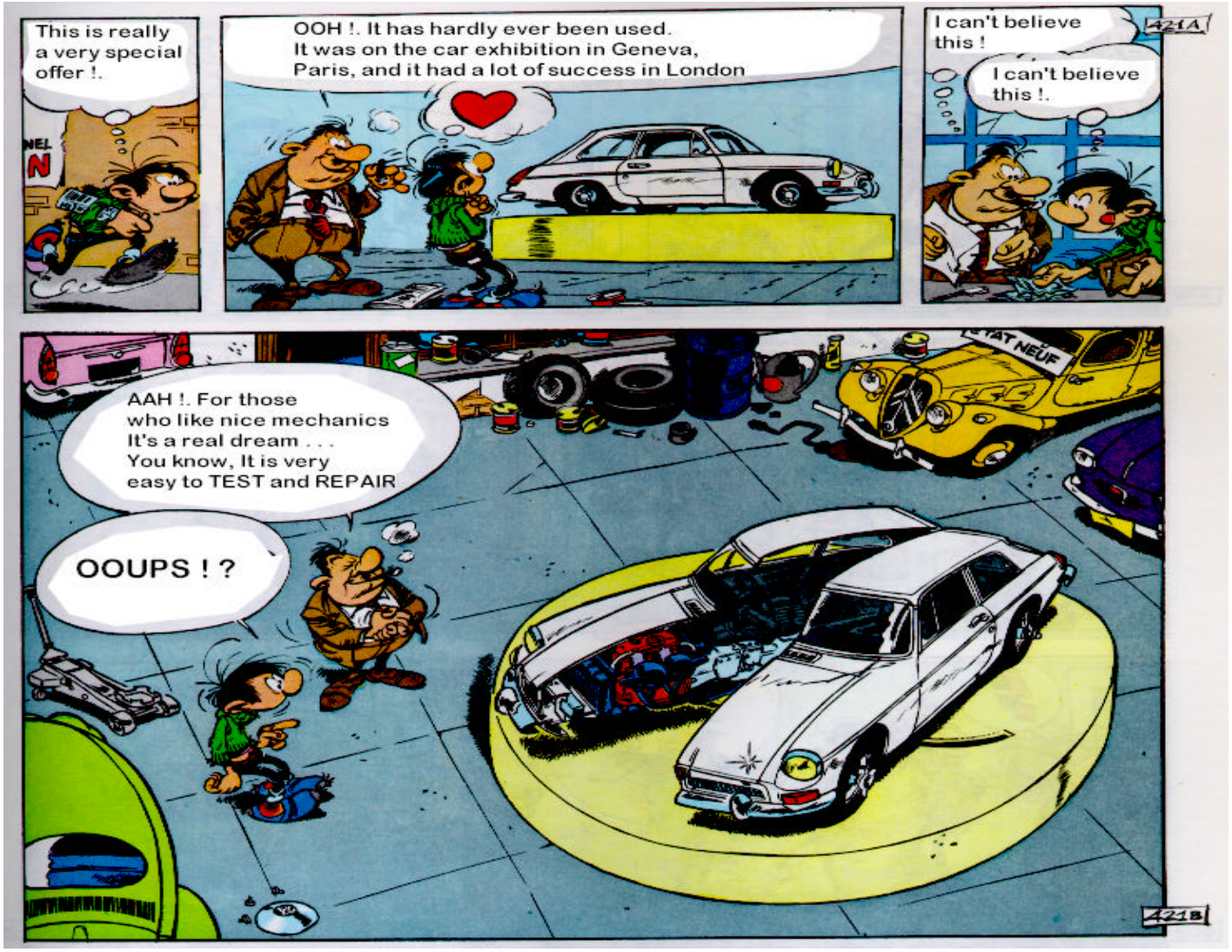


+ Measurements of DC characteristics

No standard Mixed signal tester exists (mixed signal tests are always special)

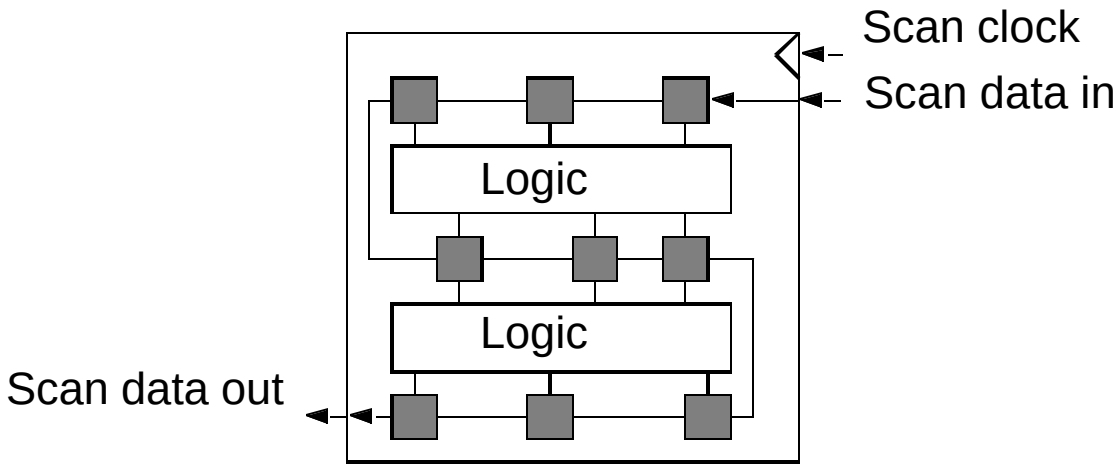
Testers must be faster than current IC technology !.

Scan Path testing



Scan path testing

Improving controllability/observability by enabling all storage nodes to be controlled/observed via serial scan path.



Test principle:

1: Enable scan mode and scan in control data.
2: Disable scan mode and clock chip one cycle.
3: Enable scan mode and scan out observing data.

Generation of test vectors: With the high controllability/observability the test vectors can be generated automatically with a ATPG program.

JTAG standard

IEEE 1149 standard.

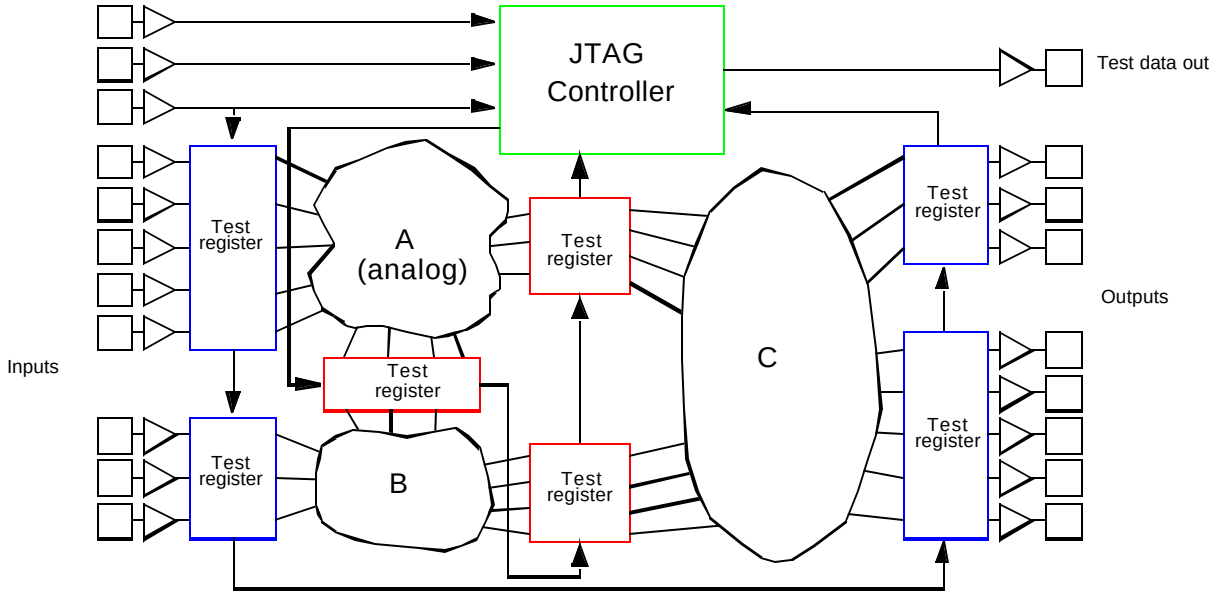
Boundary scan to test interconnect between chips.

Internal scan to test chip.

Control and status of built in self test.

Chip ID

Many commercial chips with JTAG standard implemented:
Processors, FPGA, etc.



Boundary scan enables test of digital board connections.
(automatic test generation from netlist of board)

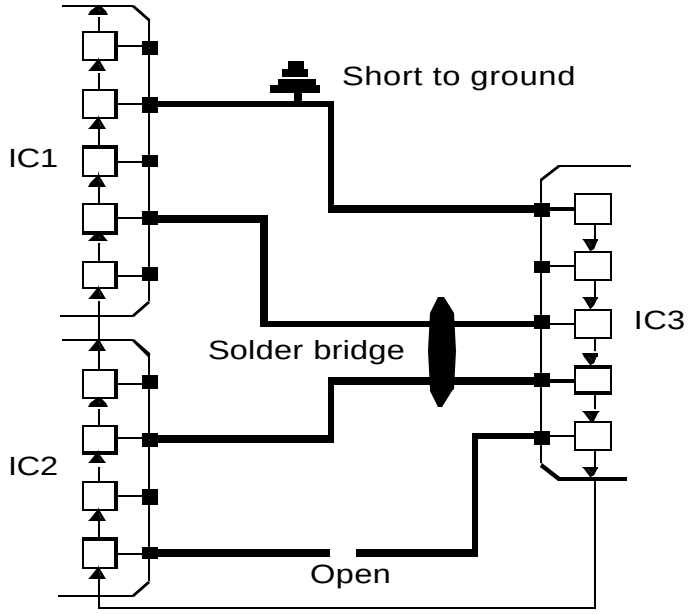
JTAG ID enables verification of correct component type.

Enables access to internal test features in components.

Testing can be also be performed in-situ.

Small and “cheap” test system required.

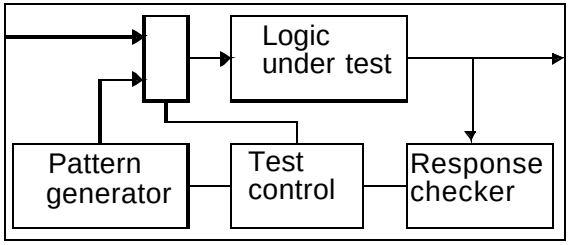
Many commercial IC’s now have JTAG (Processors, FPGA’s, etc.)



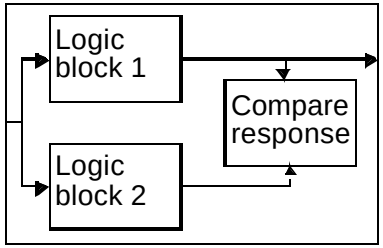
Built In Self Test (BIST)

Different schemes of built in (self) test

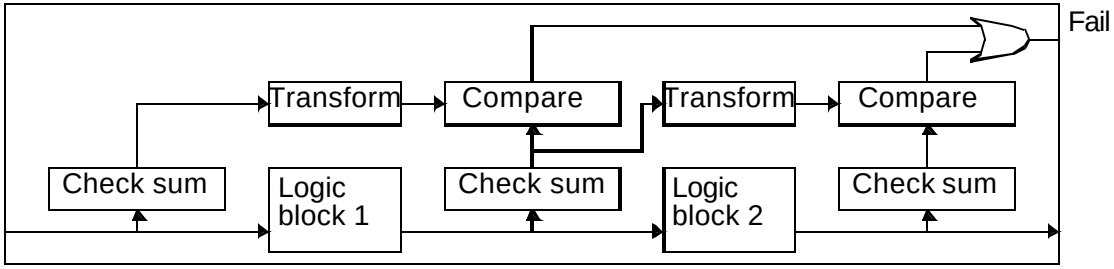
Include test pattern generator and response check on chip



Make self checking during operation by duplicating all functions



Generate local check sums and check with transformation of previous check sum



Hardware overhead !!

Trends in IC design

J. Christiansen
CERN - EP/MIC
Jorgen.Christiansen@cern.ch

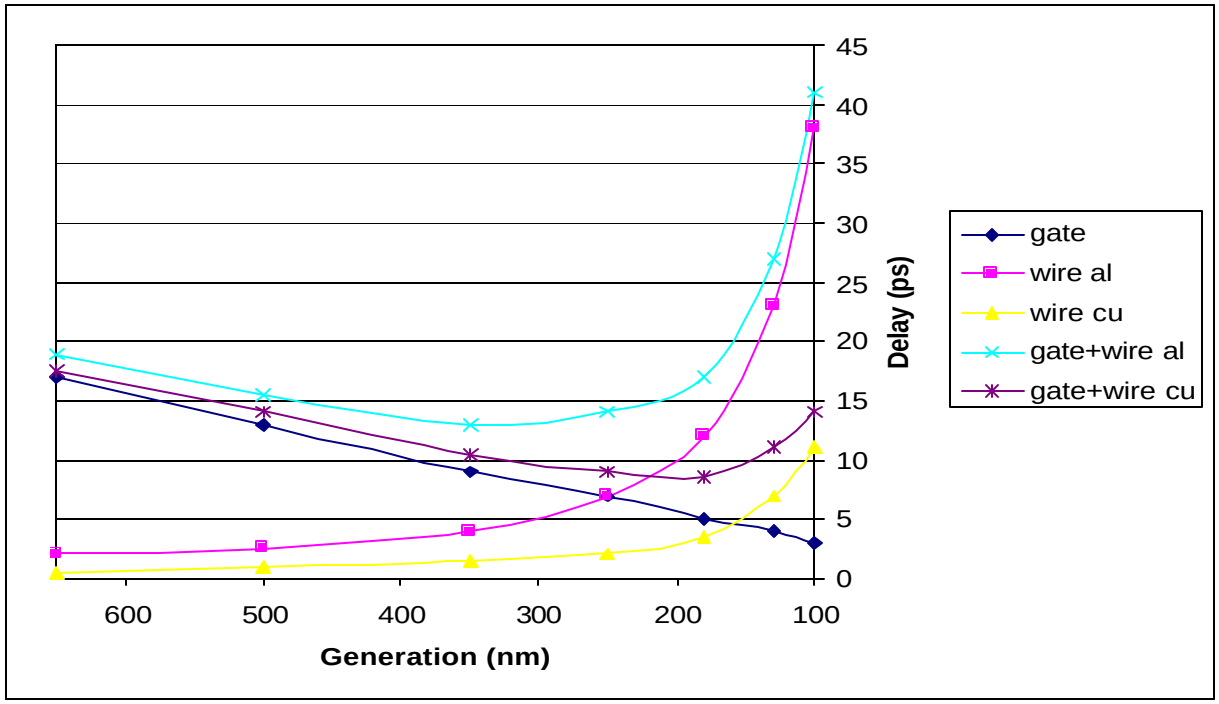
SIA CMOS Roadmap (from 1997, old)

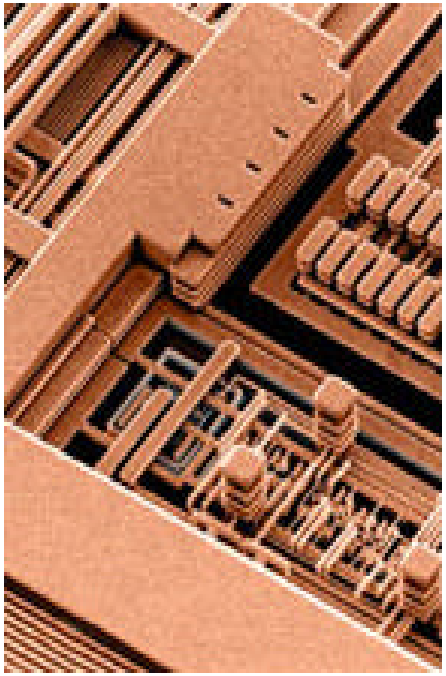
	1997	1999	2001	2003	2006	2009	2012
Technology							
Technology	.25 µm	.18 µm	.15 µm	.13 µm	.10 µm	70 nm	50 nm
Gate Delay Metric *CV/I* [7]	16-17 ps	12-13 ps	10-12 ps	9-10 ps	7 ps	4-5 ps	3-4 ps
Overall Characteristics							
Logic transistor density	3.7 M/cm^2	6.2 M/cm^2	10 M/cm^2	18 M/cm^2	39 M/cm^2	84 M/cm^2	180 M/cm^2
DRAM size	256M	1G	1G	4G	16G	64G	256G
DRAM IC size	170 mm^2	240 mm^2	270 mm^2	340 mm^2	480 mm^2	670 mm^2	950 mm^2
MPU chip size	300 mm^2	340 mm^2	385 mm^2	430 mm^2	520 mm^2	620 mm^2	750 mm^2
MPU pin count	800	1000	1200	1500	2000	2600	3600
MPU clock frequency	750 MHz	1.2 GHz	1.4 GHz	1.6 GHz	**2.0 GHz**	2.5 GHz	3 GHz
ASIC clock frequency	300 MHz	500 MHz	600 MHz	700 MHz	900 MHz	1.2GHz	1.5GHz
Power supply voltage	1.8-2.5V	1.5-1.8V	1.2-1.5V	1.2-1.5V	.9-1.2V	.6-.9V	.5-.6V
MPU high power	70 W	90 W	110 W	130 W	160 W	170 W	175 W
MPU low power	1.2W	1.4W	1.7W	2W	2.4W	2.8W	3.3W

Solutions Exist **Solutions Being Pursued** **No Known Solution**

Gate and wire delay

- Gate delay decreases
- Wire delay increases
- Copper wires required to take advantage of decreased gate delay
- Place and route critical



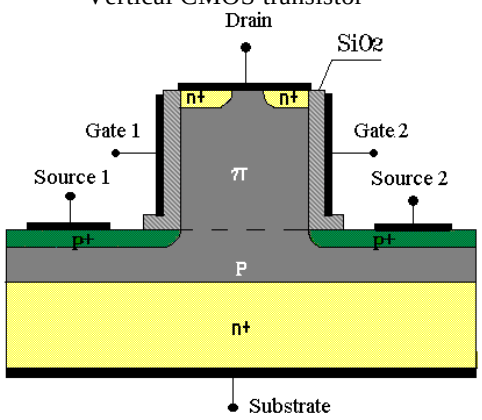


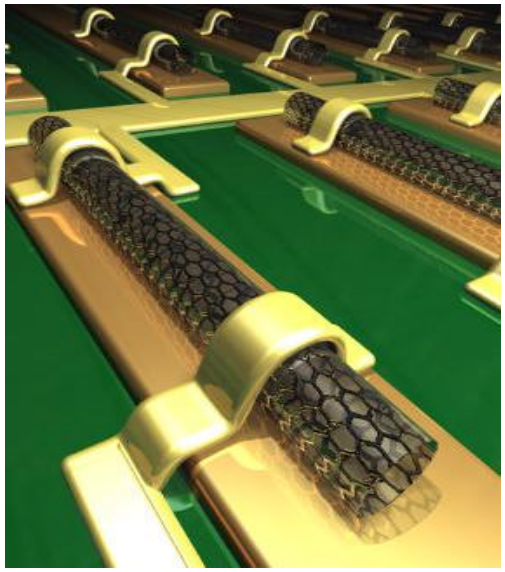
Technology

- Developing new technologies are increasingly expensive
  - Significant changes in fabrication needed for deep sub-micro technologies:
    - Deep UV lithography with reflective optics or
    - E-beam or
    - X-ray
- Large companies forced to make strategic alliances to finance development of new technologies
    - IBM, Infinion, UMC
    - ST, Phillips, Motorola
    - Others

- CMOS technology changes:
  - Ever decreasing device sizes (higher integration and faster)
    - When will it all end ? 50nm ?
  - Decreasing power supply voltage
  - Copper interconnect
  - Low dielectric constant insulation materials to decrease interconnect capacitance (but hard to exchange SIO_2)
  - Silicon On Insulator (SOI)
  - Vertical and/or 3D transistors
- Which technology(ies) will take over after CMOS ?
  - Molecular devices ?
  - Quantum devices ?
  - Carbon nano tube devices ?
  - Optical devices ?
  - Single electron transistors ?

Vertical CMOS transistor





Nanotube transistor

Production facilities

- About 10 fabs open per year
- Fab Cost ~2 B$
  - Affordable only for DRAM and very high volume companies
  - Fab-less companies (e.g. Xilinx)
- Technology lifetime 4-5 years
- Completely new fab. needed for next generation technology
- The microelectronics industry is known to have its up and downs (~5 year period) but still continuously increase in value. This makes it hard to plan investments in fabrication facilities

Design

- Most designs will be based on synthesis except memory, analog and special devices.
- Analog design will become increasingly difficult because of decreased power supply voltage and change of transistor characteristics.
  (the world is going digital but is at its origin analog)
- Place and route will become (is) the critical tool.
- Crosstalk between digital signals must be taken into account
- High performance tools will be needed for design and verification
- High performance tools will stay expensive and will probably become even more expensive.
- Design and prototyping costs will increase
- New architectures to take advantage of increasing number of transistors (e.g. Vector processing, VLIW)