Improving Transition Delay Fault Coverage Using Hybrid Scan-Based Technique*

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ABSTRACT

This paper presents a hybrid scan-based transition delay fault test. The proposed technique controls a small subset of scan cells by launch-off-shift method and the rest by launch-off-capture method. An efficient ATPG-based controllability measurement approach is proposed to select the scan cells to be controlled by launch-off-shift or launch-off-capture. In this technique, local scan enable signals are generated on-chip using two local scan enable generator cells. The cells can be inserted anywhere in a scan chain and the area overhead is negligible. The launch and capture information of scan enable signals are transferred into the scan chain during scan-in process. Our technique improves the fault coverage and reduces the pattern count and the scan enable design effort. The proposed hybrid technique is practice-oriented and implemented using current commercial ATPG tools.

I. INTRODUCTION

Modern ICs are growing more complex in terms of gate count and operating frequency [1]. The deep-submicron (DSM) effects (higher clock rate, shrinking geometries, longer wires, etc.) are becoming more prominent, thereby increasing the probability of timing-related defects [2] [3]. The stuck-at fault model [4] alone is not capable of catching timing- or speed-related defects in modern day designs and cannot ensure high quality level of chips.

In the past, functional patterns were used for at-speed test. However, functional testing is not a viable solution because of the difficulty and time to generate these tests for complex designs with very high gate density. On the other hand, functional testing may require a large test sets for large circuits to achieve a desirable fault coverage. Therefore, more robust at-speed techniques are required as the number of timing-related defects is growing and effectiveness of functional and I_{DDQ} testing is reducing [5] [6].

Transition fault and path delay fault are two prevalent fault models and together provide a relatively good coverage for delay-induced defects [7] [8]. The transition fault model targets each gate output in the design for a *slow-to-rise* and *slow-to-fall* delay fault while the path delay model targets the cumulative delay through the entire list of gates in a pre-defined path [9]. Transition fault model is widely practiced when compared to path delay fault model and commercial tools are available for computing such tests.

A. Scan-Based Transition Fault Test

Scan-based structural tests are increasingly used as a cost-effective alternative to the at-speed functional pattern approach [6] [10]. To perform a transition fault test, a pattern pair $(V1, V2)$ is applied to the circuit-under-test (CUT). Pattern $V1$ is termed as the initialization pattern and $V2$ as the launch pattern. $V2$ launches the signal transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) at the desired node. The response of the CUT to the pattern $V2$ must be captured at functional speed (rated clock period). The whole operation can be divided into 3 cycles: 1) Initialization Cycle (IC), where the CUT is initialized to a particular state ($V1$ is applied), 2) Launch Cycle (LC), where a transition is launched at the target gate terminal ($V2$ is applied) and 3) Capture Cycle (CC), where the transition is propagated and captured at an observable point.

Transitions can be applied in different ways to CUT. There are three different ways to test transition faults, which are called *Launch-off-Shift* (LOS) or *Skewed-Load* [11], *Launch-off-Capture* (LOC) or *Broad-Side* [12] and *Enhanced Scan* [13]. Note that, in this paper, we focus only on the first two transition test methods, i.e. LOS and LOC.

• **Launch-off-Shift (LOS):** In LOS, the transition at the gate output is launched in the last shift cycle during the shift operation. Figure 1(a) shows the path of transition launch in LOS method for a multiplexed-DFF design; similar approach can be applied to an LSSD. The transition is launched from the scan-in pin (SD) of any flip-flop in the scan chain. This activates the required transition at the target gate terminal which is propagated and captured through the functional path at an observable point (D) of any flip-flop in the scan chain.

Figure 1(a) also shows the waveforms during the different cycles of LOS operation. The LC is a part of the shift operation and is immediately followed by a fast capture pulse. The scan enable (SEN) signal is high during the last shift and must go low to capture the response at the CC clock edge. The time period for SEN to make this $1 \rightarrow 0$ transition corresponds to the functional frequency. Hence, LOS requires the SEN signal to be timing critical. Skewing the clock (CLK) creates a higher launch-to-capture clock frequency than standard shift clock frequency. Authors in [14] list more launch-off-shift approaches and waveforms.

• **Launch-off-Capture (LOC):** Figure 1(b) shows the transition launch path of the second approach, LOC method. In this method, the transition is launched and captured through the functional pin (D) of any flip-flop in the scan chain. Since, the launch

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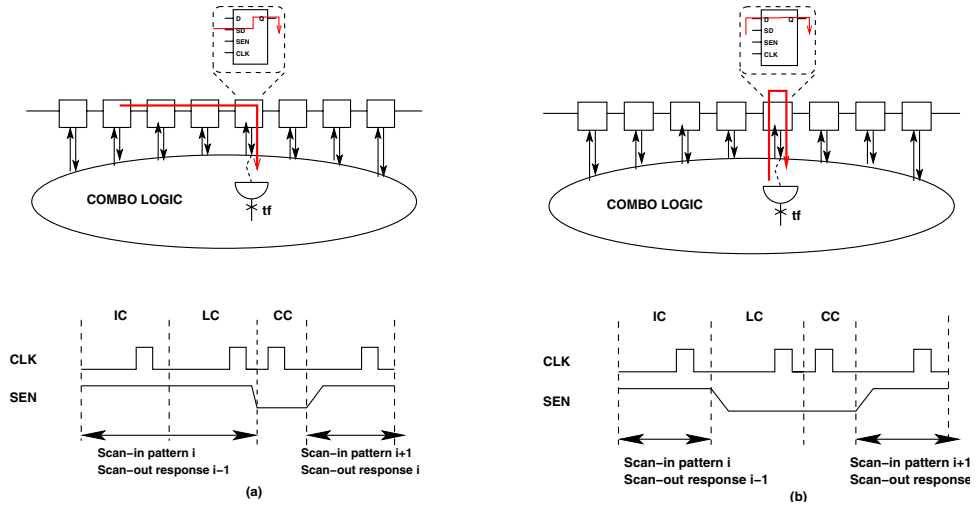


Fig. 1. (a) Launch-off-shift and (b) Launch-off-capture.

pattern $V2$ depends on the functional response of the initialization vector $V1$, the launch path is less controllable due to which the test coverage is low. Figure 1(b) also shows the waveforms of the LOC method in which the launch cycle is separated from the shift operation. At the end of scan-in (shift mode), pattern $V1$ is applied and CUT is set to an initialized state. A pair of at-speed clock pulses is applied to launch and capture the transition at the target gate terminal. This relaxes the at-speed constraint on the SEN signal and dead cycles are added after the last shift to provide enough time for the SEN signal to settle low.

• **LOS vs. LOC:** The LOS method is preferable from ATPG complexity and pattern count view points, compared to LOC method [16]. In case of LOC, a high fault coverage cannot be guaranteed due to the correlation between the two patterns, $V1$ and $V2$ ($V2$ is the functional response of $V1$). As the design size increases, the SEN fanout exceeds any other net in the design. The launch-off-shift constraints SEN to be timing critical which makes it difficult to implement using very low cost testers as well as on designs where the turn-around-time is critical. That is the main reason that LOC method has been widely practiced, especially on very low cost testers [10]. In this paper, we propose a technique to use both LOS and LOC methods in scan-based designs.

B. Related Prior Work

In [15], a hybrid scan architecture is proposed which controls a small subset of selected scan cells by LOS and the rest are controlled by LOC approach. A fast scan enable signal generator is designed which drives the LOS controlled scan flip-flops. The selection criteria of the LOS controlled scan flip-flops determines the effectiveness of the method. In some cases, the number of patterns generated by the hybrid method exceeds the LOC pattern count. Section II discusses this technique more in detail.

A restricted scan chain reordering is proposed in [20] to improve the fault coverage of skewed-load (or LOS) approach. This technique restricts the distance by which a scan flip-flop can be moved to create the new scan chain order. The scan flip-flops are reordered to minimize the number of undetectable faults due to test pattern dependency. Achieving high coverage path delay fault testing requires the application of scan justified test vector pairs, coupled with careful reordering of scan flip-flops and/or insertion of dummy flip-flops in the scan chain [21]. The authors in [21] proposed a technique considering both the number of dummy flip-flops and wirelength costs to improve path delay fault coverage.

An automatic test pattern generator (ATPG)-based scan path test point insertion technique is proposed in [22] to achieve high fault coverage for scan designs. This technique breaks the shift dependency between adjacent flip-flops by inserting dummy gates or flip-flops. The proposed technique uses a special ATPG to identify pairs of adjacent flip-flops between which test points are inserted. The authors in [23] proposed topology-based latch correlation measures and used by companion latch arrangement algorithm to guide the placement of latches in a scan-based design to minimize the effect of correlation and maximize the fault coverage of delay faults.

C. Contribution and Paper Organization

In this paper, we propose a new hybrid scan-based technique to improve the fault coverage of transition fault test. The proposed hybrid scan architecture controls a small subset of selected scan cells by LOS and the rest by LOC method. An efficient ATPG-based controllability measurement approach is proposed to select scan cells to be controlled by LOS or LOC method. The selection criteria is to improve the fault coverage of transition test and reduce the overall pattern count. As mentioned above, a small number of scan cells are LOS-controlled, hence only a small subset of scan chains' scan enable signals need to be timing closed resulting in reduced SEN design effort. The proposed method is robust, practice-oriented and implemented using existing commercial tools [18], i.e. no special ATPG is required unlike other hybrid techniques. Note that, in this paper, we do not explore whether the additional detected faults are functionally detectable. This is part of our future work.

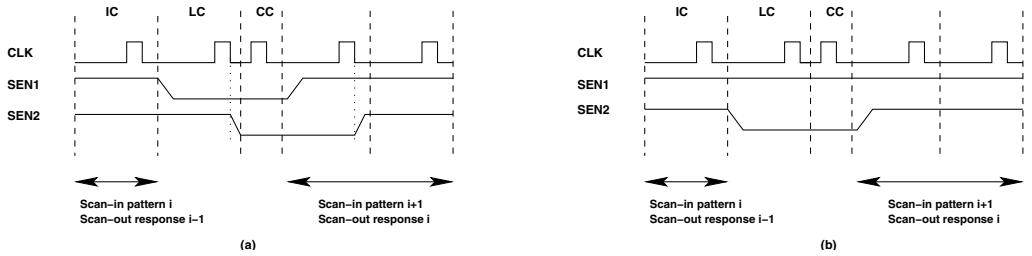


Fig. 2. (a) SEN waveforms in the hybrid-scan technique and (b) SEN waveforms in ELOC technique.

To control the scan chain mode of operation (LOS or LOC), two new scan cells, called local scan enable generators (LSEG), are proposed to generate the local scan enable signals. The scan enable control information for the launch and capture cycles are embedded in the test data itself. The LSEG cells have the flexibility to be inserted anywhere in the scan chain and the hardware area overhead is negligible.

The rest of the paper is organized as follows. Section II briefly reviews hybrid scan and enhanced LOC techniques. An ATPG-based controllability measurement is described in Section III. Section IV describes the local scan enable generation technique and operation of the LSEG cells. The scan insertion and the test pattern generation flow on an industrial design are discussed in Section V. The experimental results are presented in Section VI. Finally, concluding remarks are in Section VII.

II. Review

In this section, we review two transition fault test techniques. First technique is hybrid scan proposed in [15] which is based on using LOS and LOC approaches and the second technique is called Enhanced LOC [19] which uses LOC and scan path methods.

A. Hybrid Scan

In [15], hybrid scan architecture is proposed which controls a small subset of selected scan cells by LOS and the rest are controlled by LOC technique. The technique selects M scan flip-flops that can be driven by the scan enable without a strong buffer or buffer tree based on the highest 0 or 1 controllability measure. The 0(1) controllability measure of a line, measured using SCOAP technique [24], is the minimum number of primary and state inputs to be specified to set the line to 0(1). There is a limitation of this method as a scan flip-flop with a very high 1 controllability measure but very low 0 controllability measure will likely be selected as a LOS-controlled flip-flop since the cost is determined as $max\{C0, C1\}$. However, if the ATPG tool assigns 0s in most of the test patterns, selecting this scan flip-flop as LOS-controlled flip-flop will not help in test pattern reduction.

The internal fast scan enable generator which controls the LOS-controlled flip-flops requires one initialization cycle before starting the scan shift operation. Any internal fast scan enable transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) occurs at the negative edge of the clock cycle. It takes one additional clock cycle to revert back to shift mode after the fast capture because of the synchronous nature of the fast scan enable signal. This will corrupt the captured data in the scan chains. Moreover, the LOS-controlled flip-flops cannot be used in LOC mode. Figure 2(a), generally, shows the SEN signal waveforms of the hybrid technique that uses both LOS and LOC methods. There is always a set of faults detectable in LOC mode and not detectable in LOS mode, e.g. shift-dependency untestable faults [15] [22].

B. Enhanced Launch-off-Capture (ELOC)

A new scan-based at-speed test referred to as enhanced launch-off-capture (ELOC) is proposed in [19], in which the ATPG tool deterministically determines the transition launch path either through a functional path or the scan path. The technique improves the controllability of transition fault testing, improves fault coverage and it does not require the scan enable to change at-speed. **The internal scan enable signals do not change between the launch and capture cycles (held constant at either 0 or 1) and any scan enable transition is at shift frequency**.

Figure 2(b) shows SEN signal waveforms in ELOC technique. SEN of a subset of scan chains stays at 0 (SEN1) during launch and capture cycles to launch the transition only. The remaining scan chains are controlled using the second SEN signal (SEN2) to launch a transition through the functional path during launch cycle and capture the response during the capture cycle. Figure 3 shows a circuit with two scan chains, one acting as a shift register and the other in the functional mode. The transitions in the top scan chain are launched through the functional path while the transitions from the bottom scan chain are launched from the scan path. The conventional LOC method may be viewed as a special condition of the enhanced LOC (ELOC) method, where the scan enable signals of all the chains are '0' during the launch and capture cycles.

The scan enable control information for the launch and capture cycle is encapsulated in the test data and transferred during the scan operation to generate the local scan enable signals during the launch and capture cycle. A new scan cell, referred to as local scan enable generator (LSEG), is inserted in the scan chains to generate the local scan enable signals. The LSEG cell has the flexibility to be inserted anywhere in the scan chain and the hardware area overhead is negligible. Moreover, as the local scan enable generator flip-flops are in the scan chain, the added hardware is completely testable (detected-by-simulation).

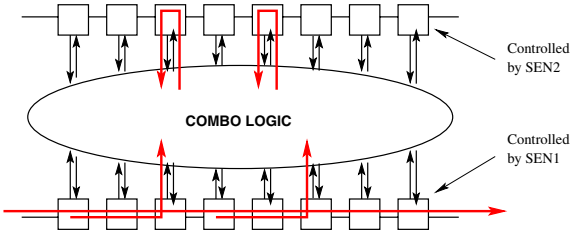


Fig. 3. Controllability of Enhanced LOC.

III. ATPG-Based Controllability Measurement

The controllability measure of a scan flip-flop is defined as the percentage of patterns, in the entire pattern set, for which a care-bit is required in the scan flip-flop, to enable activation or propagation of a fault effect. The controllability is determined by two factors: 1) the fault activation path and 2) the output logic cone driven by the scan cell. In LOS technique, the fault activation path (scan path) is fully controllable from the scan chain input. While, in LOC, the controllability of launching a transition at the target gate is less as it depends on the functional response of the circuit under test (CUT) to the initialization vector (V_1). Hence, LOS provides a better controllability which results in better fault coverage and less pattern volume than LOC technique.

The output logic cone driven by a scan flip-flop is a parameter which can be potentially used to determine the scan flip-flops in the design that require greater controllability in order to achieve higher fault coverage. A scan flip-flop driving a large output logic cone requires higher controllability than a scan flip-flop driving a smaller logic cone, to achieve the same fault coverage for a smaller pattern set.

The initialization pattern (V_1) in a transition fault test pattern pair (V_1, V_2) is essentially an IDDQ pattern to initialize the target gate to a known state. The next time frame, pattern V_2 is a stuck-at-fault test pattern to activate and propagate the required transition at the target node to an observable point. Therefore, to find the controllability measure of a scan flip-flop, we use an ATPG tool to generate stuck-at patterns and force the tool to fill don't-care (X) value for scan flip-flops which are not used in the activation/propagation of any fault. The controllability of a scan flip-flop is measured as the percentage total number of patterns for which a care-bit is required in the scan flip-flop. We, then, use the measured controllability factor of each scan flip-flop as a cost function to select the LOS-controlled flip-flops. The ATPG-based controllability measure technique overcomes the limitation of SCOAP based method used in [15], in which there is a possibility to select a scan flip-flop whose 0(1) controllability is high but not controlled to 0(1) during pattern generation by the ATPG tool.

IV. Local Scan Enable Signal (LSEN) Generation

The hybrid transition fault testing method described in Section II-A provides more controllability to launch a transition but requires independent scan enable signal (SEN) for different set of scan flip-flops. Multiple SEN ports can be used, but this increases the number of pins. Note that two types of SEN signals need to be generated on-chip. The scan enable control information for the scan flip-flops differ only during the launch and capture cycles of the pattern. Hence, the low-speed scan enable signal from the external tester can be utilized for the scan shift operation and the scan enable control information for only the launch and capture cycles can be generated internally.

A. Local Scan Enable Generator (LSEG) Cells

Here, we propose two local scan enable generator (LSEG) cells to generate on-chip local scan enables using low-speed external scan enable generated by a low cost tester. Since our hybrid technique uses both LOS and enhanced LOC techniques, both fast and slow local SEN signals must be generated. In the following, we present the two LSEG cells and their operations.

• **Slow Scan Enable Generator (SSEG):** A local scan enable generator is designed in [19], to control the transition launch path of a scan flip-flop. In the rest of this paper, this cell will be referred to as the slow scan enable generator (SSEG), as the local scan enable signal does not make any at-speed transition. Figure 4(a) shows the SSEG cell architecture. It consists of a single flip-flop which is used to load the control information required for the launch and capture cycles. The input scan enable (SEN_{in}) pin which is connected to the external scan enable signal from the tester is referred to as the global scan enable (GSEN). An additional output scan enable (SEN_{out}) pin ($GSEN + Q$) represents the local scan enable (LSEN) signal. Therefore, after going to a control state *(Q)* at the end of the shift operation (GSEN is de-asserted), LSEN remains in this state as long as it is asynchronously set to 1 by GSEN. The SSEG cell essentially holds the value 0(1) for the launch and capture cycles, which is loaded at the end of the shift operation (GSEN=1).

$$LSEN = (GSEN + Q) = \begin{cases} 1 & \text{if GSEN=1} \\ Q & \text{if GSEN=0} \end{cases}$$

Table I shows the different modes of operation of SSEG cell. $GSEN = 1$ represents the normal shift operation of the pattern. When $GSEN = 0$ and $Q = 1$, $LSEN = 1$ and the scan flip-flop acts in the shift mode to launch the transitions only (*Shift-*

TABLE I

SSEG OPERATION

GSEN	FF	LSEN	Operation
1	X	1	Shift
0	1	1	Shift-Launch (No Capture)
0	0	0	Functional-Launch-Capture

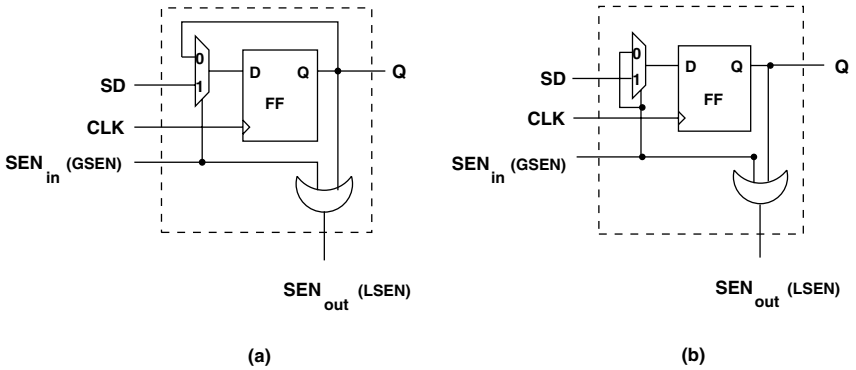


Fig. 4. (a) Slow scan enable generator (SSEG) cell and (b) Fast scan enable generator (FSEG) cell.

(No Capture) mode) and there is no capture as the LSEN signal is '1'. The capture is performed at the other observable scan flip-flops. The scan flip-flop acts in the conventional LOC method when $GSEN = 0$ and $Q = 0$ (*Functional-Launch-Capture* mode).

• **Fast Scan Enable Generator (FSEG):** A new at-speed local scan enable generator architecture, referred to as the fast scan enable generator (FSEG), is shown in Figure 4(b). Same input and output pins are considered for SSEG cell (see Figures 4(a) and 4(b)). Table II shows the different modes of operation of FSEG cell. Similar to the SSEG cell operation, $GSEN = 1$ represents the normal shift operation of the pattern. When $GSEN = 0$ and $Q = 1$, $LSEN = 1$ and the scan flip-flop acts in the (*Shift-Launch-Capture* mode) to launch the transition from the scan path and capture the response at the next capture cycle (conventional LOS method). The LSEN from the FSEG cell, makes a $1 \rightarrow 0$ at-speed transition at the launch cycle. The scan flip-flop acts in the conventional LOC method when $GSEN = 0$ and $Q = 0$ (*Functional-Launch-Capture* mode).

B. Operation of LSEG cells

The local scan enable generator cells are inserted within the scan chains and the control information is passed as part of the test data. The scan enable control information will be part of each test pattern and is stored in the tester's memory. The normal scan architecture with a single scan enable signal from the external tester is shown in Figure 5(a). There are eight scan flip-flops in the scan chain and the test pattern shifted is 10100110. The external scan enable signal from the tester is referred to as the global scan enable (GSEN). Figure 5(b) shows the same circuit in which a local scan enable signal is generated from the test pattern data for the hybrid transition fault test method. The internally generated scan enable signal is termed as local scan enable (LSEN). The main objective is to de-assert GSEN after the entire shift operation and then generate the LSEN signal during the launch and capture cycle from the test data. In this case, the pattern shifted is modified to [C]10100110, where *C* is the scan enable control bit which is stored in LSEG cell at the end of the scan operation.

The GSEN signal asynchronously controls the shift operation. GSEN is de-asserted after the *n*th shift (IC) cycle, where *n*=9. *n* is the length of scan chain after inserting LSEG cell. After the GSEN signal is de-asserted at the end of the shift operation, the scan enable control during the launch and capture cycles is the control bit *C* stored in LSEG. At the end of the capture cycle, the LSEN signal is asynchronously set to 1 by GSEN for scanning out the response. Figure 5(c) shows the process of test pattern application and also the timing waveforms for the two different local scan enable generator cells, i.e. SSEG and FSEG.

TABLE II

FSEG OPERATION

GSEN	FF	LSEN	Operation
1	X	1	Shift
0	1	1	Shift-Launch-Capture
0	0	0	Functional-Launch-Capture

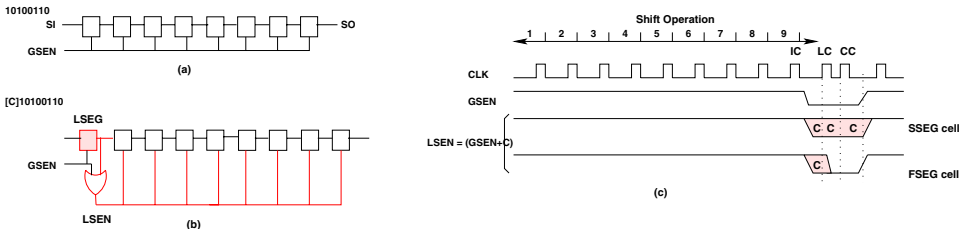


Fig. 5. (a) Scan chain architecture, (b) Local scan enable (LSEN) generation and (c) LSEN generation process.

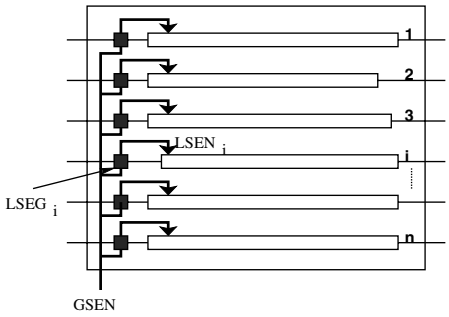


Fig. 6. Test Architecture.

V. Case Study: DFT Insertion and ATPG Flow

A. Test Architecture

The local scan enable generator based solution presented in this paper provides a method of generating the internal local scan enable signals from the pattern data and global scan enable signal from the tester. The overhead of generating the local scan enable signal is the addition of a LSEG (SSEG or FSEG) cell in the scan chain. The area overhead of an LSEG cell is a few extra gates, which is negligible in modern designs. In general, there can be multiple scan chains in a design to reduce the test application time as this is the case for today's commercial compression tools. The test application time is directly proportional to the longest scan chain length in the design. Figure 6 shows a multiple scan chain architecture with n scan chains. Each scan chain i, where $1 \leq i \leq n$, consists of an LSEG cell which generates the local scan enable signal $LSEN_i$ for the respective scan chain. The GSEN signal connects only to the SEN_{in} port of LSEG cells.

B. Case Study

In this case study, we experimented with a subchip of an industrial-strength design that had the following characteristics (Table III). The design has 16 scan chains and approximately 10K scan cells. There are 13 non-scan cells and six internal clock domains. One LSEG cell is inserted per scan chain. The test strategy is to get the highest possible test coverage for the transition faults. When generating test patterns for the transition faults, we target only the faults in the same clock domain. During pattern generation, only one clock is active during the launch and capture cycle. Hence, only faults in that particular clock domain are tested. All PIs remain unchanged and all POs are unobservable while generating the test patterns for the transition faults. This is because the very low cost testers are not fast enough to provide the PI values and strobe POs at speed.

C. DFT Insertion

As explained in Section IV, the FSEG cell generates local scan enable signal for the LOS-controlled (high controllability measure) flip-flops and the SSEG cell can enable both shift and functional launch but cannot perform capture on the flip-flops controlled in the shift-launch mode. Essentially, SSEG cell provides high controllability but less observability. In our test architecture, we control each scan chain with one LSEG cell. The type of LSEG cell used for each scan chain is determined by the average scan chain controllability measured as $\Sigma\, C_i/N$, where C_i is the controllability of ith scan flip-flop in the chain and N is the number of flip-flops in the scan chain. Figure 7 shows the algorithm used for the controllability measure based scan insertion.

TABLE III
Design Characteristics

Clock Domains	6
Scan Chains	16
Scan flip-flops	10477
Non-scan flip-flops	13
Transition Delay Faults	320884

01: Normal Scan Insertion
02: ATPG-based controllability measure of flip-flops
03: Arrange flip-flops in non-increasing order of controllability measure
04: Assign the new order of scan cells to each scan chain
05: Re-stitch scan chains with LSEG-based control for each chain

Fig. 7. Algorithm for controllability based scan insertion.

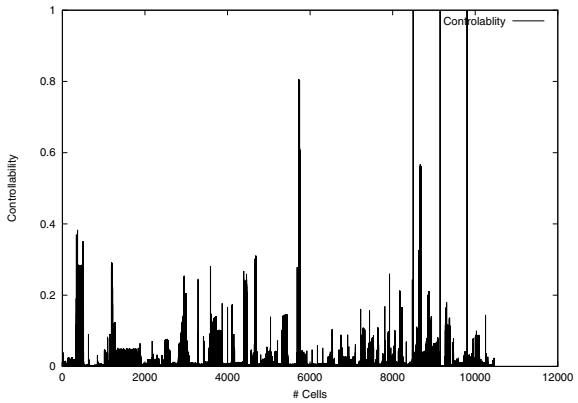


Fig. 8. Scan flip-flop controllability measure.

Figure 8 shows the controllability measure of each flip-flop measured using ATPG-based technique in our design. It can be noted, that approximately only 20-30% of the entire flip-flops require very high controllability. Hence, scan enable need not be at-speed for all scan flip-flops. Figure 9 shows the average controllablity measure of each chain for normal scan insertion and after controllability-based scan insertion. The controllability measure of the first 5 chains, as shown in Figure 9(b) is very high and the rest of the chains is very low. Therefore, the first 5 chain's scan enable signal can be designed to be at-speed (controlled using FSEG cell) and the rest of the scan chains can be controlled using the slow speed scan enable (controlled using SSEG cell).

Synopsys DFT Compiler [18] was used for scan chain insertion in the design. To insert the LSEG cells, additional commands are required during the scan chain configuration. The synthesis tool must recognize the LSEG cell as a scan cell in order to stitch it into the scan chain. This requires it to be defined as a new library cell with the scan cell attributes.

A workaround is to design the LSEG cell as a module and declare it as a scan segment of length 1. The GSEN signal is connected to all the LSEG cells SEN_{in} input pin. To insert the LSEG cells in the scan chain, one command must be used to declare the scan path including the LSEG cell. Only the LSEG cell is specified in the scan path, as the tool will stitch the rest of the cells including the LSEG cell and balance the scan chain depending on the longest scan chain length parameter. Another command is used to hookup each LSEG cell's SEN_{out} port in a particular chain to all the scan enable input port of the scan flip-flops in the respective chain.

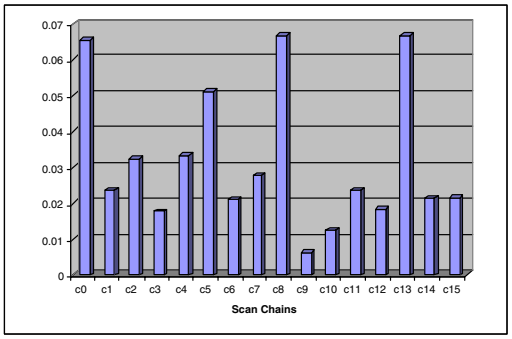
D. ATPG

The ATPG tool must be able to understand the local scan enable generation methodology and deterministically decide the transition fault activation path. Commercial ATPG tools were used for test pattern generation. A test pattern generation tool supports two ATPG modes: 1) Basic-Scan and 2) Sequential. Basic-Scan ATPG is a combinational-only mode with only one capture clock between pattern scan-in and scan-out of response while the Sequential mode uses sequential time-frame ATPG algorithm. By default, when generating test patterns for transition fault LOC method, the commercial ATPG tools use a two-clock ATPG algorithm that has some features of both the Basic-Scan and Sequential engines. The tool understands the local scan enable generation technique using LSEG cells and is able to decide the launch path for the target transition fault deterministically. Hence, there is no fundamental difference in the ATPG methodology when we use the LSEG-based solution.

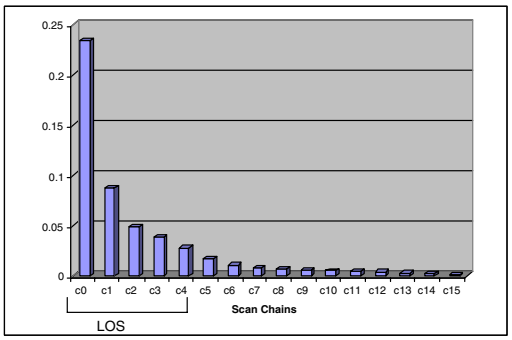
The scan enable signal for the flip-flops for the launch and capture cycles now comes from an internally generated signal. Notice that the OR gate in the LSEG cell generates the local scan enable signal through a logical OR of the global scan enable and the Q

TABLE IV
ATPG RESULTS

	Normal Scan Insertion			*Controllability-based Scan Insertion*
	LOS	*LOC*	*ELOC[19]*	*Hybrid*
Detected faults	292342	282658	288681	295288
Test Coverage	91.30	88.27	90.15	91.92
Fault Coverage	91.11	88.09	89.96	91.74
Pattern Count	1112	2145	2014	1799
CPU Time *[sec]*	329.30	896.96	924.74	1014.60



Average Controllability for Normal Scan Insertion
(a)



Average Controllability after Controllability based Scan Insertion
(b)

Fig. 9. Average controllability before and after controllability-based scan insertion.

TABLE V
CHARACTERISTICS OF FOUR MORE INDUSTRIAL DESIGNS

Design	Scan Cells	# Chains	Clocks	TF	UF	RF
A	10477	16	6	384998	64154	320844
B	29962	16	13	1066290	182622	883668
C	50342	16	3	2283636	309518	1974118
D	104539	8	1	4116092	628954	3487138

output of the flip-flop FF (see Figures 4(a) and (b)). The global scan enable signal is in active mode during scan shift operation. The tool determines the local scan enable for each chain and shifts the control value into the LSEG cell during pattern shift, used for launch and capture. It also deterministically decides the combination of scan chains to work in *Shift/Functional-Launch* mode, to activate a transition fault.

The results for conventional LOS and LOC (*Normal Scan Insertion*), Enhanced LOC (ELOC) [19] and hybrid transition-delay ATPG on this design are shown in the Table IV. We see that LOS methodology gave approximately 3% higher fault coverage than the LOC methodology. The Enhanced LOC method gives approximately 1.9% higher fault coverage compared to LOC method. The hybrid transition fault technique gives a better fault coverage when compared to LOS, LOC and ELOC methods and it also provides a better pattern count compared to LOC and ELOC methods. The pattern count is more than LOS but at the advantage of only 5 chains being timing closed for at-speed scan enable. The hybrid scan technique proposed in [15] gives, in some cases, more pattern count compared to LOC technique. The CPU time of hybrid method is greater than all other technique as the ATPG tool has to do more processing to determine the possible combinations of the SSEG controlled scan chains to work in shift register mode or in functional mode.

VI. EXPERIMENTAL RESULTS

We have experimented our technique on four more industrial designs and Table V shows the characteristics of these designs. In all designs, each scan chain is inserted with one LSEG (SSEG or FSEG) cell. The total transition faults are shown in column *TF*. During ATPG, the faults related to clocks, scan-enable and set/reset pins, referred to as untestable faults (*UF*), are not added to the fault list. The clock related faults can only be detected by implication and the remaining faults (scan-enable/set/reset) are untestable as the signals remain unchanged during the launch and capture cycles. These faults contribute approximately 10-15% of the total transition faults. The total transition faults excluding *UF* faults is used as the real fault (*RF*) set during pattern generation.

Table VI shows the ATPG results comparing LOS, LOC, ELOC and hybrid methods. The FC and # Patt columns shows the fault coverage percentage and the number of patterns generated respectively for each method. The ELOC method provides

TABLE VI

ATPG RESULTS FOR EIGHT INDUSTRIAL DESIGNS.

Design	*LOS*			*LOC*			*ELOC [19]*			*Hybrid*		
	FC (%)	# Patt	CPU Time *[sec]*	FC (%)	# Patt	CPU Time *[sec]*	FC (%)	# Patt	CPU Time *[sec]*	FC (%)	# Patt	CPU Time *[sec]*
A	91.11	1112	329	88.09	2145	896	89.96	2014	924	91.74	1799	1014
B	87.94	4305	3569	85.14	8664	7800	86.57	8539	8702	88.03	8062	6611
C	81.10	6869	8415	79.42	12073	22930	80.48	11583	25642	83.29	8134	14451
D	92.15	5933	6559	91.56	10219	12088	92.28	12505	47788	94.83	9674	18410

fault coverage up to 1.87% (ΔFC) compared to LOC method. The ELOC gives an intermediate fault coverage and pattern count between LOS and LOC. The hybrid method provides a better coverage compared to all other methods, as it has the flexibility to use combinations of functional and scan path for launching a transition. It provides higher fault coverage up to 2.68% and 3.87% compared to LOS and LOC, respectively. The number of patterns for hybrid method is slightly higher than LOS method and lower than both LOC and ELOC methods. Note that the CPU time for hybrid and ELOC method is greater than LOC method since the tool has to do additional processing to find the transition launch activation path.

VII. CONCLUSION

We have proposed a hybrid technique to improve the transition delay fault coverage and reduce the pattern count. The proposed technique used both LOS and LOC methods by using two cells. The cells generate the local scan enable signals. One cell generates a fast scan enable and another generates the slow scan enable signal. Both cells are simply tested using flush patterns during testing scan flip-flops. There are some faults that LOS method can detect but LOC cannot and vice versa. Using both techniques in the proposed hybrid scan resulted in increasing fault coverage. An ATPG-based controllability measurement was proposed to select the LOS- and LOC-controlled scan cells. The technique was implemented on a number of industrial designs. The experimental results show up to 3.87% increase in fault coverage over LOC achieved with lower number of patterns. The proposed technique increases the CPU runtime to generate the test patterns, this is mainly due to the process of finding the scan cells suited to be controlled for LOS or LOC.

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