

INDEX

- architecture body, 4
- ASCII code, 177, 194
- ASM chart, 108
- ASMD chart, 128
- barrel shifter, 62
- BCD, 147
- binary decoder, 43, 45, 48–49
- case statement, 49
- CLB, 13
- component instantiation, 6
- conditional signal assignment, 41
- constant, 53
- constraint file, 23
- Core Generator, 245
- counter, 81, 96
- D FF, 71
- data type, 3
 - enumerated, 111
 - signed, 37
 - std_logic, 3, 39
 - std_logic_vector, 4
 - two-dimensional array, 79
 - unsigned, 37
- DCM, 239
- DDR register, 239
- debouncing circuit, 118, 132
- development flow, 15
- division circuit, 143
- edge detector, 114
- entity declaration, 3
- FIFO buffer, 100, 171
- flag FF, 169
- floating-point adder, 63
- FSM, 74, 107
- FSMD, 74, 127, 324
- generic mapping, 55
- generics, 54
- hold time, 72
- HyperTerminal, 177, 194, 208
- identifier, 3
- if statement, 47
- instruction memory, 324
- instruction ROM, 329, 363
- instruction set, 329
- interrupt, 341, 405
- IOB, 239
- KCPSM3, 328, 332, 342, 345, 359
- logic cell, 11
- logic synthesis, 16
- LUT, 12, 243
- macro cells, 13
- maximal operating frequency, 73
- Mealy output, 108
- memory controller, 215, 220, 244
- mode
 - in, 3
 - inout, 40
 - out, 3
- Moore output, 107
- multiplexer, 41, 44

- operator
 - arithmetic, 37
 - concatenation, 38
 - logical, 4
 - relational, 37
- package
 - numeric_std, 37
 - std_logic.1164, 3, 79
 - std_logic_arith, 38
 - std_logic_signed, 38
 - std_logic_unsigned, 38
- pad delay, 234
- PBlazeIDE, 332, 342, 359
- placement and routing, 16
- priority encoder, 41, 44, 48–49
- process, 46
- program counter, 324
- PS2
 - keyboard, 188
 - mouse, 200
 - receiver, 184
 - transmitter, 201
- RAM
 - block, 244, 282, 292
 - distributed, 243
 - dual-port, 249, 283, 298
 - single-port, 246
 - static, 215–216
- register, 72, 77
- register file, 78, 100, 222
- register transfer methodology, 35
- register transfer operation, 127
- regular sequential circuit, 74
- ROM, 251, 274
 - font, 292
- RS-232, 163
- selected signal assignment, 44
- sensitivity list, 46
- sequential statement, 46
- setup time, 72
- shift register, 79
- sign-magnitude adder, 59
- slice, 13
- state diagram, 108
- static timing analysis, 16
- structural description, 6
- synchronous design methodology, 71
- technology mapping, 16
- testbench, 8, 28, 84
- tri-state buffer, 39, 220
- type conversion, 37
- UART, 163, 386
- ucf file, 23
- VGA mode, 260
- video memory, 282
- video synchronization, 260