Defect detection by the bulk current

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Abstract:

Start-up experiences with a new test method for VLSI-circuits similar to I_{DDQ}[1]-test will be presented. The evaluation of the power supply current is replaced by the observation of the bulk current. It avoids the obstacles of on-chip I_{DDQ}-test, the loss of performance due to the current sensor in the power supply line or the huge bridging transistor for the current sensor. The results, based on process and device simulation, show the potential defect detection features and the feasibility of the new test method.

0 Introduction

The idea to use the quiescent bulk current to test a circuit makes use of the excellent defect detection properties of I_{DDQ}-test and tries to avoid basic problems of checking for a defect indicating power supply current. I_{DDQ}-test is the additional monitoring of the decay of the power supply current in each test step. It uses the property of CMOS-circuits that the power supply current fades away after each charge/discharge process. In a CMOS gate consisting of an n-channel and a complementary p-channel network only one of the two networks should be conductive simultaneously. The power supply current returns almost to zero. A significant increased current indicates a defect, e.g. a short or a defective transistor. The main advantage of I_{DDQ}-test is that it is sensitive to defects which are difficult to catch during logical testing [1], [2], [3] and defects that indicate early failures [4]. Optimistic forecasts assume that I_{DDQ}-test enables the reduction of the defect level of CMOS circuits by one or two orders of magnitude [2].

The first section of the paper deals with advantages and problems of I_{DDQ}-test. A bulk current measuring is only feasible with an on-chip current sensor. The second section discusses some aspects of using I_{DDQ}-test in a built-in self-test environment. The defect detection features of the bulk current are discussed in section 3 at the device level and in section 4 at the gate level. Section 5 introduces the concept of a bulk current measurement unit.

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[1] I_{DDQ} - quiescent power supply current

1 Quiescent power supply current measurement

The measurement equipment for the quiescent power supply current test is charged with problems. The I_{DDQ} of a defect-free gate is in the order of magnitude of a few nanoampere or less. It is noticeable higher than the quiescent current of a defective gate. But in a VLSI-circuit, the leakage currents of many thousand defect-free gates adds up. To check for the low error current of a single gate the circuit under test has to be divided into multiple blocks with separate current monitoring. In normal operation the measurement unit has to be bridged. Otherwise, the current sensor changes the input and output levels of the circuit and reduces the speed of operation.

To detect a current of a few nanoampere it needs a resistor of some magaohm in the power supply line. An additional capacity of *1 pF*, which is not much for the whole net of power supply lines and thousands of gates, increases the measuring time by microseconds. The reduction of the capacities per measuring arrangement is the second reason to divide the circuit into blocks with a separate current sensor [5].

The quiescent current check must wait until all in-circuit recharging processes are finished. The quiescent time differs from test step to test step and is effected by production tolerances. A too short time between switching of input signals and measuring of the current causes a risk to classify defect-free circuits as defective ones. On the other hand the time for testing shouldn't be excessive long what leads to a trade-off.

2 Quiescent power supply current monitoring in a built-in self-test environment

The quiescent bulk current is much lower than the quiescent power supply current of a defective gate. To measure it needs an on chip current sensor. The idea is obvious to use it in a built-in self-test environment. For I_{DDQ}-test too, the combination with a built-in self-test architecture is advantageous.

Some problems mentioned above can be avoid with the self-test arrangement according to Fig. 1 [6]. The current sensor, the base-emitter junction of a bipolar transistor operating in grounded emitter configuration, is integrated on the chip. A parallel connected resistor adjusts the switching threshold. The signal "*current floats"/"doesn't float*" is measured in amplified

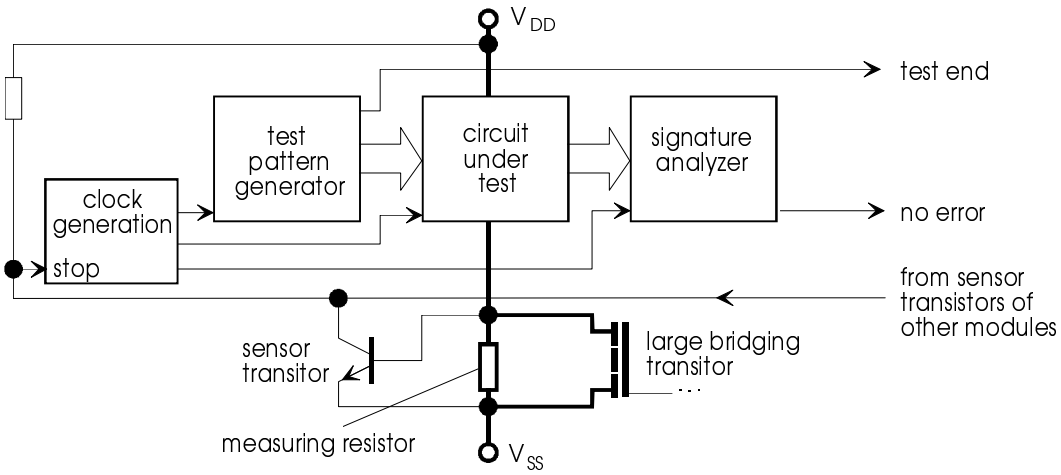

Fig. 1: I_{DDQ}-test in a built-in self-test environment

form at the collector. This kind of sensor is fast and sensitive. The long measuring time due to the high capacities of the circuit and low thresholds for the error current will be obtained by dividing the circuit under test in a large number of blocks with separate current monitors. The sensor transistors of all modules form a wired-OR.

The time between switching of input signals and measuring the power supply current is adjusted by a link between the current sensor and the clock of the test arrangement. The clock of the test pattern generator, the unit under test and test data analysis circuitry switches only after the power supply current has fallen below the error threshold. The minimal test time adjusts automatically. In the case of a defect the test arrangement does not produce an end signal. The test time of a defect free circuit, which is the sum of all measuring delays, is an indicator for technological problems (e.g. changed film resistances).

In normal operating the measuring transistor has to be bridged. This is the most critical part of the test arrangement. The peaks of the power supply current of a VLSI circuit may exceed 1 *A* during switching operation. The resistance of the bridging transistors in the on state must be extremely low. Very broad transistors are necessary. Altogether, the bridging transistors may cost 3 to 10% of the whole chip area [7]. This makes the integration of the quiescent power supply current sensor expensive.

3 Sources of the quiescent bulk current

The bulk current in a MOS-transistor originates from capacitive currents, leakage currents and generation currents. Changing levels at the transistor terminals (source gate and drain) and changing levels at wires crossing the well of a transistor cause capacitive currents. They disappear after each switching operation and do not produce a quiescent bulk current. Measurable leakage currents in CMOS-circuits originate from defects (e.g. gate oxide shorts and defective pn-junctions in the source/drain regions). The third source, the generation current is also sensitive to defects. It disappears in a defect free CMOS-circuit after each switching operation. As it will be shown in the following, a static generation current is sensitive to similar defects as the I_{DDQ}. Only the generation current will be discussed in the following.

The generation current is a parasitic effect originating in the pinch-off region of the characteristic curve of a MOS-transistor. Assuming a n-channel transistor, a voltage between gate and bulk greater than the threshold voltage V_{Th} produces a conductive channel at the surface of the substrate. A current through the channel causes a potential gradient between channel and gate and the potential gradient a gradient in the development of the channel. If the voltage between gate and drain is lower than the threshold of the transistor, the conductive channel ends near the drain region. The channel is pinched off. The length of the pinch-off region adjusts automatically by its voltage drop corresponding to the difference between the source-drain voltage and the threshold voltage. Because of the high field strength the charge carriers in the pinch-off region are accelerated beyond the normal drift speed and by impact ionisation with the lattice atoms additional change carrier pairs are generated. In a n-channel transistor the produced electrons are attracted by the drain and the holes flow mainly to the bulk (Fig. 2 left). The charge carrier generation is nearly proportional to the field strength and the current in the pinched-off region. Fig. 2 shows at the right side the characteristic curve of the bulk current generation of a n-channel transistor. The generation of p-channel transistors is similar.

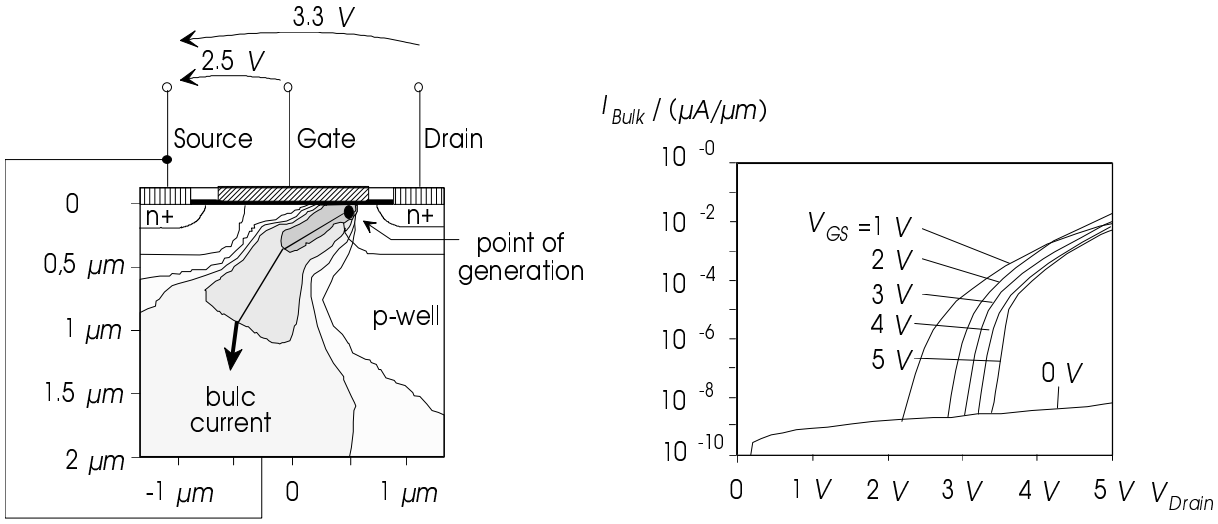

Fig. 2: Bulk current generation in a n-MOS transistor and the characteristic curve of the generation current (simulated by ZANAL [9])

4 Error detection behaviour

The two conditions for a bulk current generation are a current in the channel, and that the channel is pinched-off. After all recharging processes have settled, there is no current through any of the transistors in a defect-free. The bulk current caused by the generation is zero. Many defects not detectable by logical testing manifest themselves as forbidden voltages on input terminals of a gate. Fig. 3 shows the characteristic generation curve of an inverter. Up to reaching the threshold voltage of the n-channel transistor this one is switched-off. Current flows neither through the n- nor through the p-channel transistor. No bulk current is generated. Increasing the input voltage up to near the switching point, the n-channel transistor is pinch-off and generates a bulk current of a few *pA* per μm transistor width. After exceeding the switching point up to the cut-off of the p-channel transistor the p-channel transistor is pinched-off and generates a bulk current. So, almost each wrong input voltage at the input terminal causes a generation current in one of the transistors. This property holds also for complex logical gates, if the static current flows through the pinched-off transistor. In contrast to I_{DDQ}-test the bulk current test does not detect wrong input voltages equal to the switching voltage of the gate.

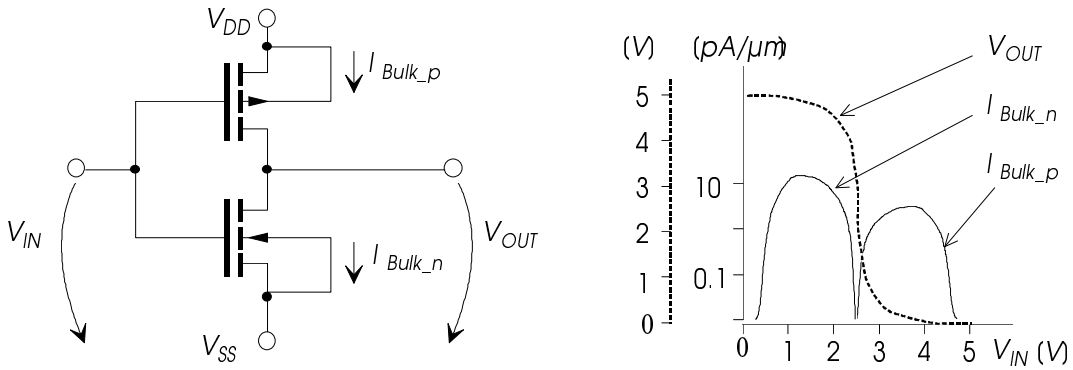

Fig. 3: Bulk current generation in dependence on the input voltage of an inverter

One of the main defect sources in integrated circuits are shorts [8]. A short is only detectable if the shorted nodes are connected simultaneously by switched-on transistor-limbs with the ground and the power supply. A simplified model is an inverter with the gate of the n-channel transistor linked to the power supply line and the gate of the p-channel transistor to ground (Fig. 4). Normally, in CMOS-technology the threshold-voltages of the n-channel and the p-channel transistors are approximately equal by value. Under this assumption, a short causes a generation current in one of the transistors, if the common voltage of the shorted node is either lower than the threshold or higher than the power supply voltage minus the threshold. In other words, a short causes a bulk current generation in one of the upstream transistors if the common voltage corresponds to a low or high, which it will do in general (Fig. 4). Conductive transistors have a strong non-linear characteristic curve. A slight difference in the current richness (v) between the conductive n-channel and the conductive p-channel transistor limb causes a common high or low level. Only, if the characteristic curves of both transistor limbs have the same shape ($v \approx 1$), the short causes a voltage between high and low (an forbidden voltage). Forbidden voltages are observable by generation currents in downstream gates. Bridges to the power supply and ground lines are also detectable by generation currents either in the upstream device (low resistive shorts) or via a wrong voltage at an input of a downstream device (high resistive shorts) [7].

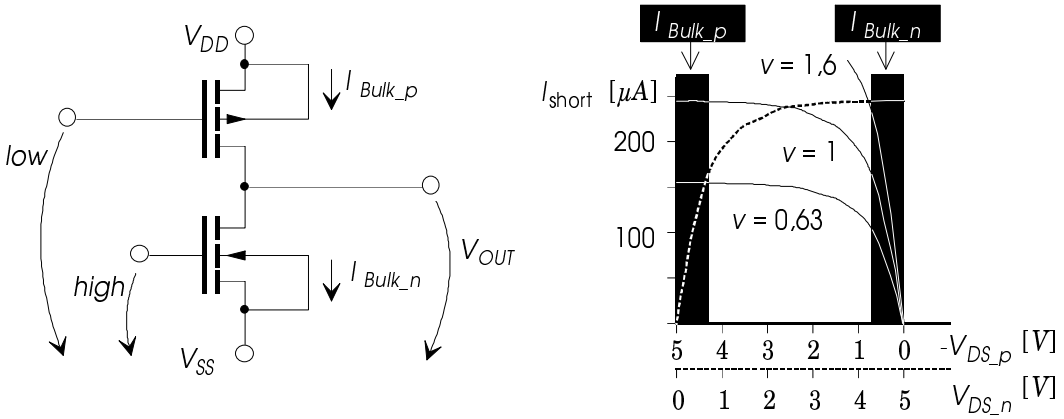

Fig. 4: Bulk current generation of shorted signal lines

The defect-indicating bulk currents are very sensitive to the power supply voltage. For voltages of 3 *V* and lower, no generation currents are observable. The lower bound for testing is a power supply voltage of about 5 *V* to 6 *V*.

5 Built-in bulk current monitoring

The rate of quiescent bulk current indicating a defect is only some *pA* or less. Because of the large capacities, a direct measuring of the currents from the wells would be very slow. A proper solution is to place additional minimum size transistors in the wells which are used as bipolar amplifiers for the bulk current. The following explanation relates to n-channel transistors in p-wells. In the test mode the well is conducted by n+-areas instead by the normal p+-well contacts (Fig. 5). This contact operates as emitter of the sensor transistor. The basis of the sensor transistor is the well and the basis current is the bulk current from the MOS transistors. The amplified current will be measured at the collector which has a much lower capacity than the well. The amplified bulk currents of different wells are summed up before evaluation. The rest of the test arrangement corresponds to Fig. 1.

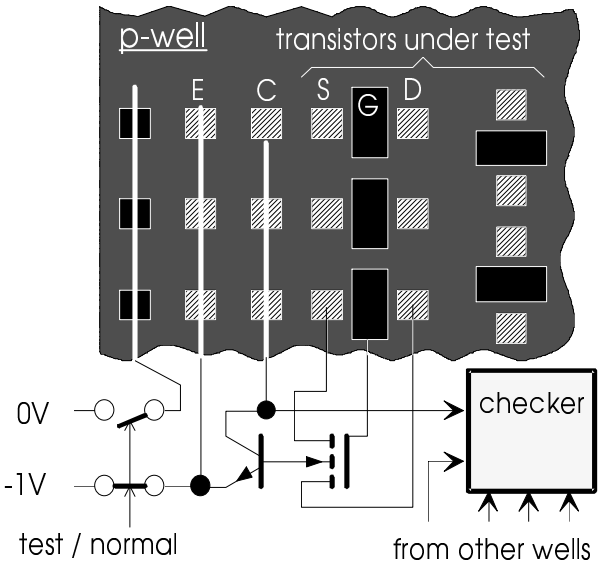

Fig. 5: Measuring arrangement to check for an increased bulk current

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