Exercise 2: PS/2 keyboard

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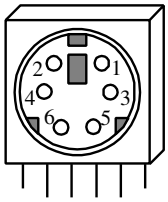
May 22, 2012

Abstract

First a simple given receiver for PS/2 data packages has to be checked with the logic analyzer. Afterward the function should be improved.

1 PS/2 protocol

The FPGA board has a 6-pole mini-DIN connector to plug in a PS/2 keyboard or a PS/2 mouse (figure 1).



Pin	Function
1	Data
2	Reserved
3	GND
4	Vdd
5	Clock
6	Reserved

Figure 1: Connector to plug in PS/2 devices

PS/2 defines a synchronous serial protocol (see figure 2). Each PS/2 data package consists of 11 bits

- 1 start bit (zero)
- 8 data bits
- 1 parity bit (odd parity)
- 1 stop bit (one)

which are after another submitted via the the same wire. An additional clock signal informs the receiver, when the data bits are valid.

if there is no transmission the data and the clock line are one (start bit). The transmission starts with a falling edge of the data line to zero. A time T_{SU} later the clock first changes to zero an has in total 11 falling and 11 rising edges.

The times between clock edges must be in the interval:

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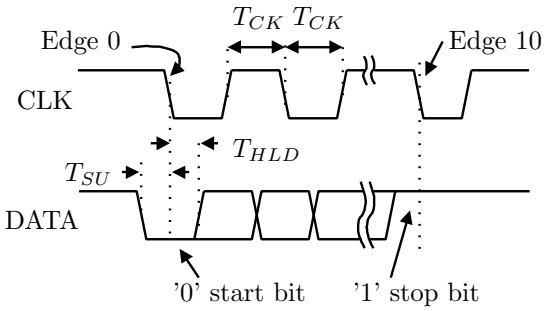

Figure 2: PS/2 Protokoll

Symbol	Parameter	Min.	Max.
T_{CK}	duration of the clock period	30µs	50µs
T_{SU}	setup time data must be stable before a clock edge	5µs	25µs
T_{HLD}	hold time data must be stable after a clock edge	5µs	25µs

With the second falling edge bit(0), with the 3. edge bit(1) etc. up to with the 9. clock edge bit(7) is on the bus. The parity bit, witch must be on the data line during the 10th clock edge, is calculated as follows:

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P<=not(D(0) xor D(1) xor D(2) xor D(3) xor
       D(4) xor D(5) xor D(6) xor D(7));
```

It is used for transmission error detection. During the last rising edge the data wire has to be one (stop bit).

2 Key codes

In the exercise the scan codes of a PS/2 keyboard should be read and displayed. Each key has its own scan code (figure 3), which the keyboard sends if a key is pressed. Pressing longer the scan code is sended multiple times (approximately every 100 ms). Releasing a key the code "F0" followed by the scan code is transmitted.

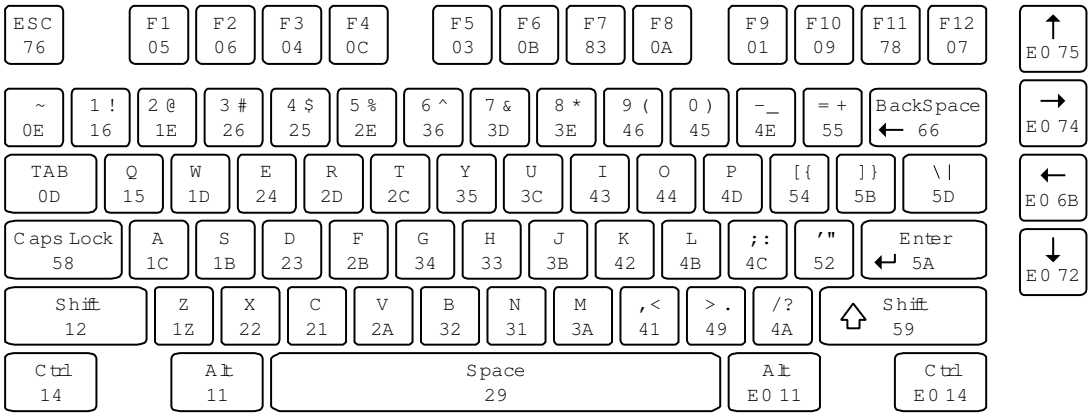

Figure 3: PS/2 keyboard scan codes

3 Experiment

Copy the files a2_ps2.xise, a2_ps2.vhd and a2_ps2.ucf in a new directory and open the project with ISE. The file a2_ps2.vhd contains a simple receiver for PS/2 data packages. It consists of:

- a process, that samples the data and the clock signal of the PS/2-Bus with a frequency of 100 kHz
- an 11 bit shift register that stores the sampled data withe the sampled PS/2 clock.

The eight sampled bits are displayed e.g. the last sampled scan code are displayed on latches.

- Compile the project
- program it on the FPGA board.
- plug in a keyboard
- Note in a table (on a sheet of paper) five scan codes for five different keys and compare it to figure 3.
- Why the sign "F0" (key released) does not become visible on the LEDs?

4 Check the data with the logic analyzer

In the file a2_ps2.vhd the PS/2 clock file and the PS/2 data signal are led to pins on the daughter board are connector A2 (clock to pin "DB0", data to pin "ADR1"). Connect the logic analyzer to those pins an start measurement using the file a2_ps2.xml.

To visualize the code "F0" followed by the scan code after releasing a key requires a bit of luck. Adapt the trigger condition so that measurement starts after releasing the key.

5 Improve the circuit

A Disadvantage of the circuit so fare is, that LEDs flicker when new data arrive. The circuit should be substituted by an automaton that only updates the LED output after transmission has finished and no errors are detected. Proposed solution:

1. The initial state should be S0
2. In S0: wait on a falling edge on the sampled data; change to state S1. If the clock wire doesn't stay zero, error LED should be switched on.
3. In S1: wait on a falling edge on the on the sampled clock; change to state S2.
4. In Si ($i \in \{2, 3, \ldots, 9\}$: wait on a falling edge on the sampled clock; increase state number by one; concatenate the sampled data bit to the bit vector in the shift register
5. In S10: wait on a falling edge on the sampled clock, copy the sampled date in an output signal parity; change to state S11.
6. In S11: wait on a falling edge on the sampled clock; change to initial state.

To check for protocol errors an 8 bit error counter should be added and increased by one when

1. in S0 if sampled clock is not ≫1≪
2. in S1 if sampled data is not ≫0≪
3. in S10 if received parity is wrong and

4. in S11 if sampled data is not ≫1≪.

5. In S12: wait on a falling edge on the sampled clock;

The scan code and the value of the error counter should be displayed on the 7 segment display (reuse exercise 3 from part 1 of the lab course).

6 Additional task

Extend the automaton so that it detects, if a button is pressed ore released. It should be displayed on an additional LED.

7 Check list for the compliance test

- to be able to present the measurement with the logic analyzer and to explain the resulting waveform
- working receiver circuit without flickering LEDs.