Lecture 3: Asynchronous Input Signals

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Asynchronous input signals, at the test board the signals from the switches and buttons, has to be sampled before internal processing with a clock period larger than the de-bouncing time (see [1], section 1.5). The following exercises introduce step by step the design of a sequential circuit with asynchronous inputs from switches and buttons.

1 Examination of the bouncing of a switch with the logic analyzer

Program the FPGA so that the switch input »SW0« on the test board is connected via the FPGA with LED »LD0« and pin 5 of expansion connector »A2« (LOC D5) (figure 1 a). Connect the logic analyzer as shown in figure 1 b and record the waveform during turning the switch on several times (Settings for the logic analyzer: 1.500.000 samples per second, trigger on first rising edge of the signal). How long is the maximum observed bouncing time? By which power of two the 50 MHz clock should be divided to sample the switching signal?

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity Draht is
 Port (x : in  STD_LOGIC;
  y, led : out STD_LOGIC);
end entity;
architecture a of Draht is
begin
 y   <= x;
 led <= x;
end architecture;
```

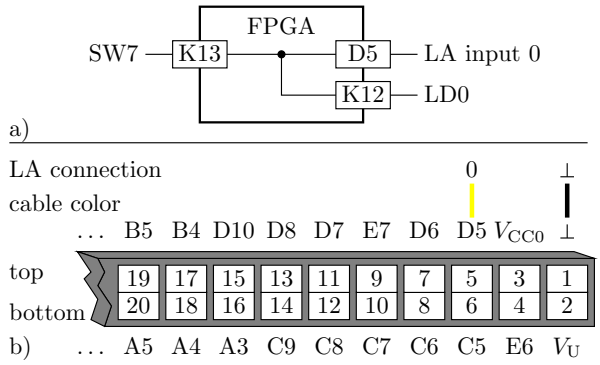

Figure 1: a) Circuit for exercise 1 b) Connection of the logic analyzer to the expansion connector »A2« (Draht – engl. wire)

2 Counting the signal edges during bouncing

For this experiment the sequential circuit in figure 2 a has to be described in VHDL and programmed in the FPGA. The switching signal is sampled by a shift register of length two. If both values differ the counter state is increased by one. The counter state is displayed on the LEDs.

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The circuit description consists of a sample process with the clock in the sensitivity list, in which with every rising edge the input signal is assigned to the first shift register bit »SW7_del« and the first shift register bit is assigned to the second shift register bit »SW7_del2. The "+"-operation is overloaded in the package »IEEE.STD_LOGIC_UNSIGNED«, provided by »ISE«. The clock »Clk« is the 50 MHz input clock.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_UNSIGNED.all;
entity Test_Ct is
 port (Clk, SW7: in  STD_LOGIC;
  LD : out  STD_LOGIC_vector(7 downto 0));
end entity;
architecture a of Test_Ct is
 signal SW7_del, SW7_del2: STD_LOGIC;
 signal s: STD_LOGIC_VECTOR(7 downto 0);
begin
 process (Clk)
 begin
  if RISING_EDGE(Clk) then
   SW7_del  <= SW7;
   SW7_del2 <= SW7_del;
   if SW7_del /= SW7_del2 then
    s <= s + 1;
   end if;
  end if;
 end process;
 LD <= s;
end architecture;
```

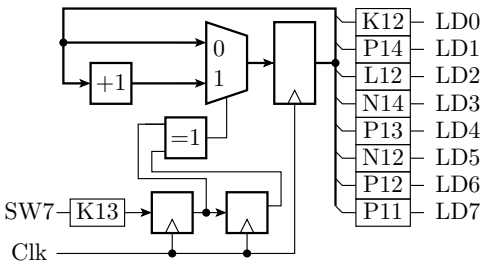

Abbildung 2: a) Circuit for the second exercise b) VHDL program

3 Clock divider

How many bits must have a clock divider to produce approximately a one Hertz clock? Describe a 24 Bit clock divider by using the template for a counter in the previous exercise. The highest eight bits should be connected to the LEDs on the test board and the 16 lower bits to the expansion connector A2 to which the logic analyzer is connected (figure 3).

- Check by observing the LEDs that the right bit position is selected for the one Hertz clock.
- Let the logic analyzer record the counter values starting from 0xa3. For this an appropriate xml-file has to be written.

4 Light effect circuit

Design a self-defined light effect circuit with switches as inputs and LEDs as outputs. The sample process should use the clock frequency determined in exercice 1 and the process to calculate the next state and the LED output with approximately 1 Hertz. An appropriate function would be circular moving light point that changes moving direction by turning a switch on, e.g. to forward by turning on »SW0« and backward by turning on »SW1«. The circuit should react on each turn on, even if the switch already has been turned off before the next rising edge of the 1 Hertz clock.

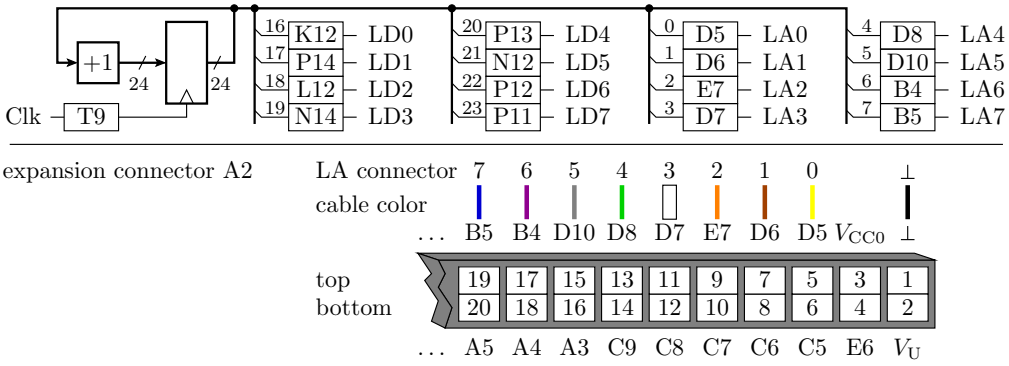

Figure 3: Clock divider

5 Check list for the compliance test

to section 1:

- a screen shoot of the waveform of the logic analyzer
- the estimated value of the maximum bouncing time
- a reasonable estimation of the sample frequency for de-bouncing

to section 2:

- the experimental determined maximum bouncing count per switching activity

to section 3:

- the counter index of the 1 Hertz clock
- a screen shoot of the recording of the logic analyzer

to section 4:

- a presentation of the light effect circuit

References

[1] G. Kemnitz. *Technische Informatik Band 2: Entwurf digitaler Schaltungen.* Springer, 2011.