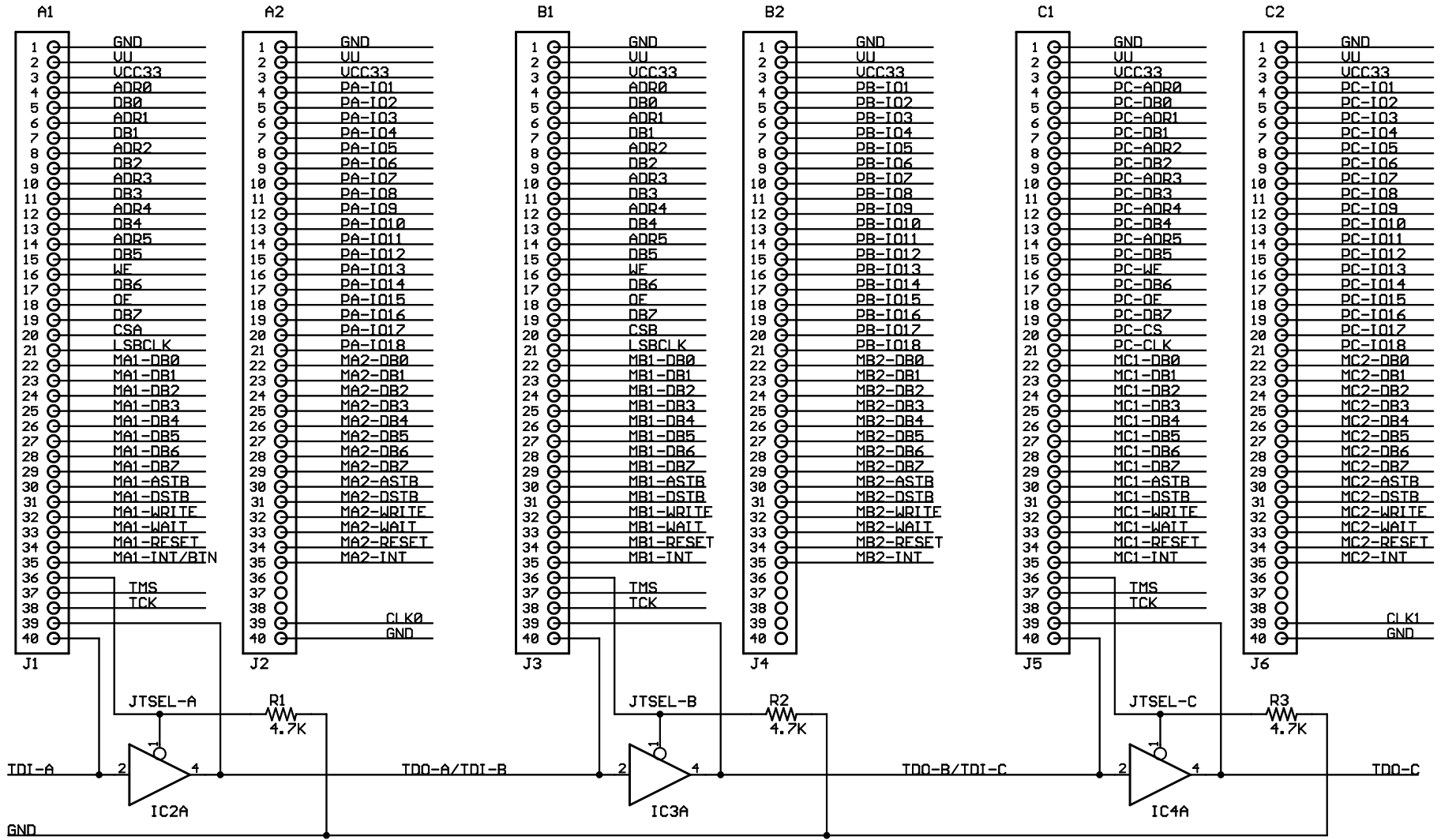


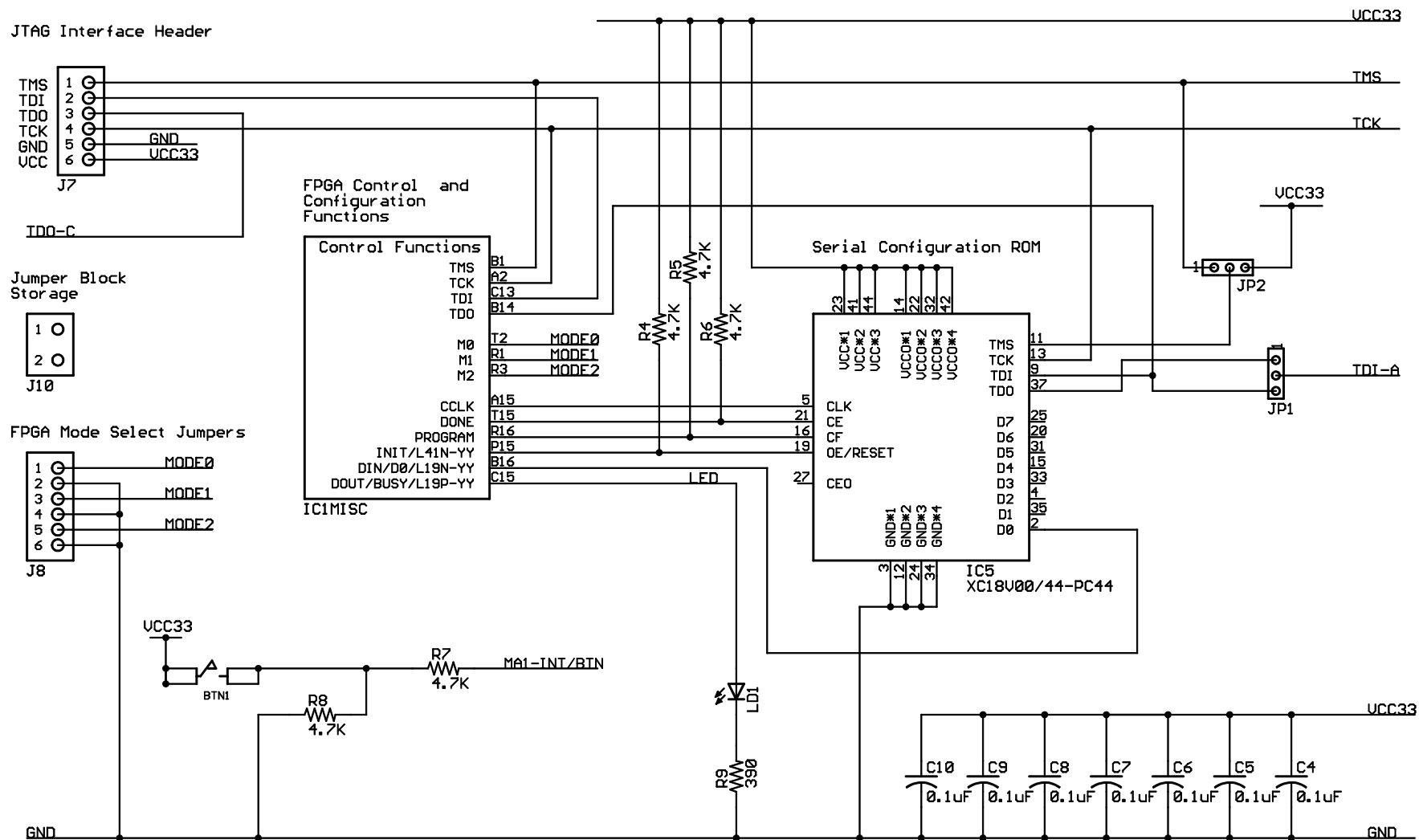
Peripheral Position A

Peripheral Position B

Peripheral Position C



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Notes: A shorting block must be installed between TDI and TDO on J7 to complete the scan chain when the JTAG signals are being driven from a peripheral board position rather than the JTAG Interface Header

Shorting blocks are installed on pins 2-3 of JP1 and JP2 to bypass the the serial configuration rom (IC5).

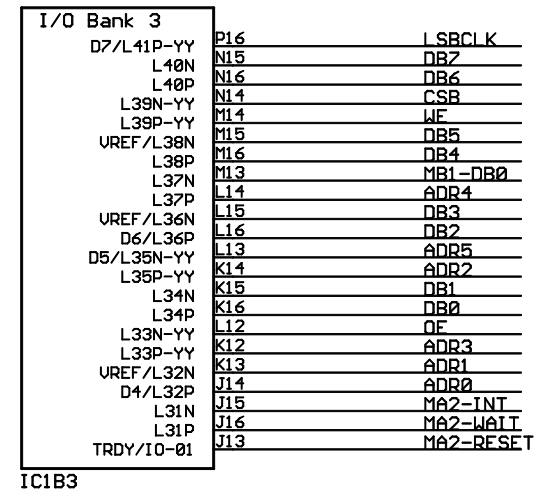
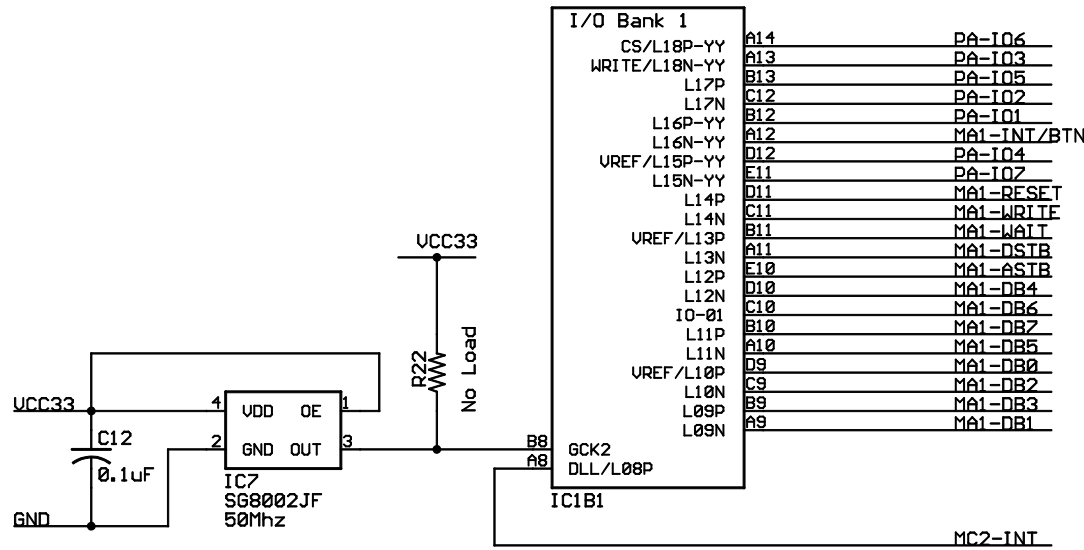
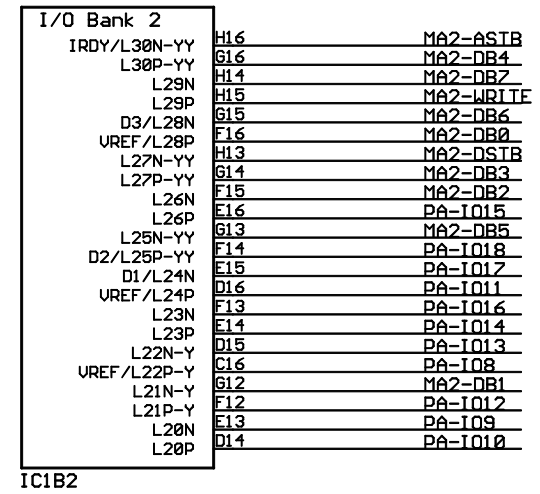
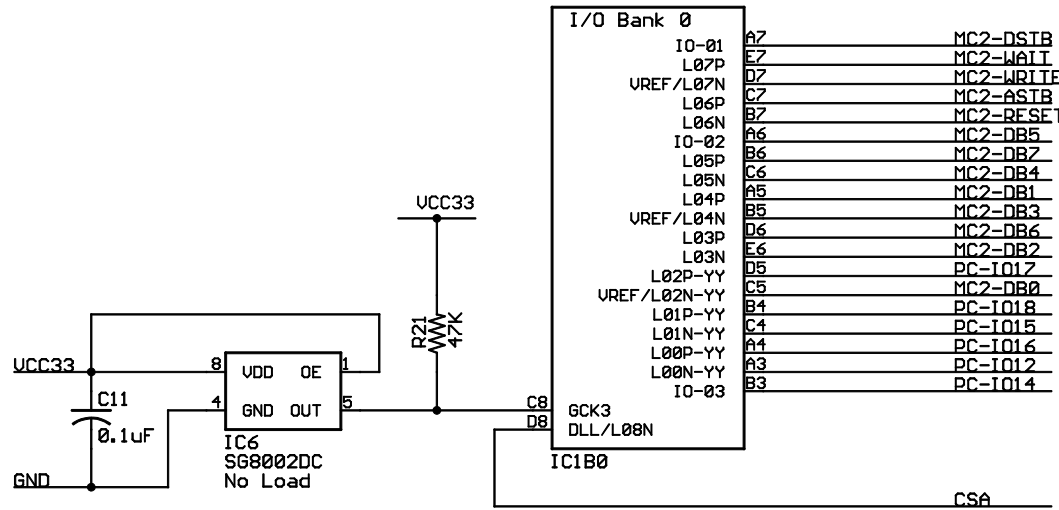
Shorting blocks should be installed on MODE0 and MODE1 of J8 to select Slave Serial Mode when configuring from the ROM

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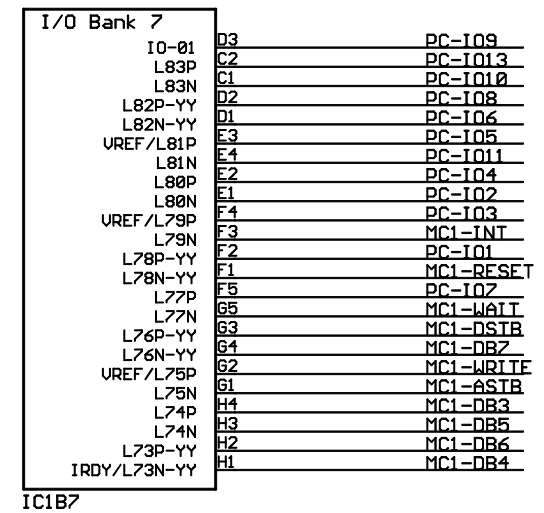
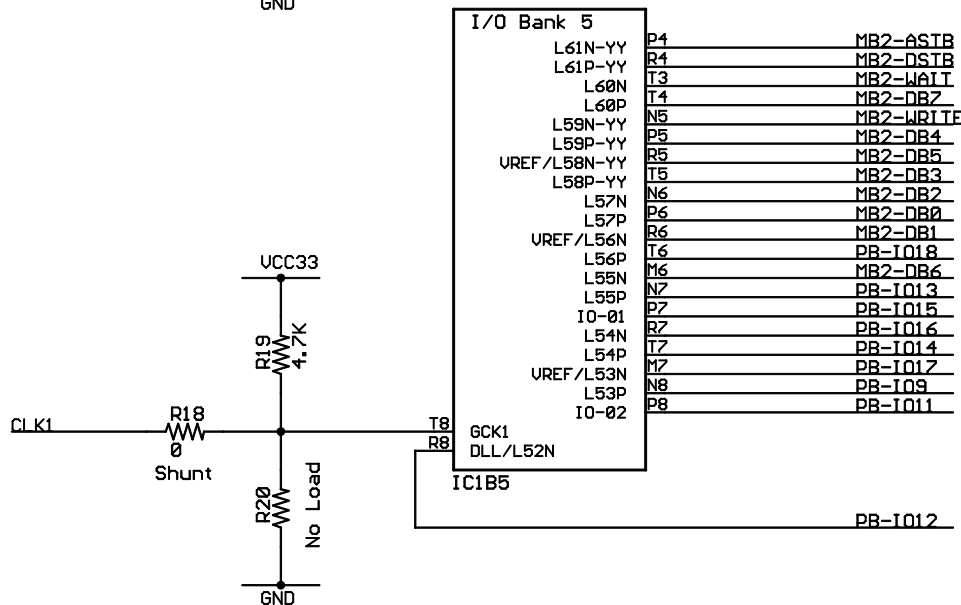
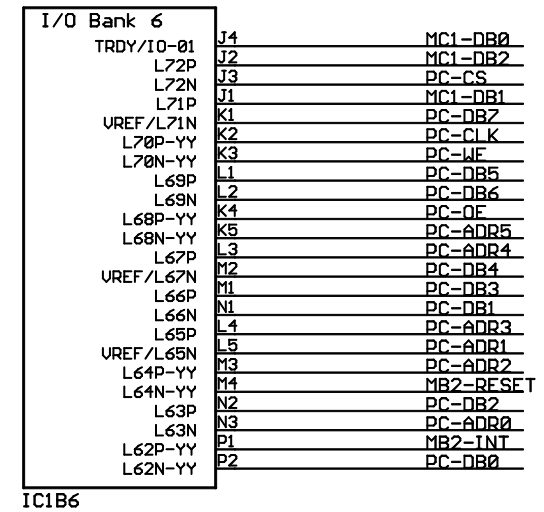
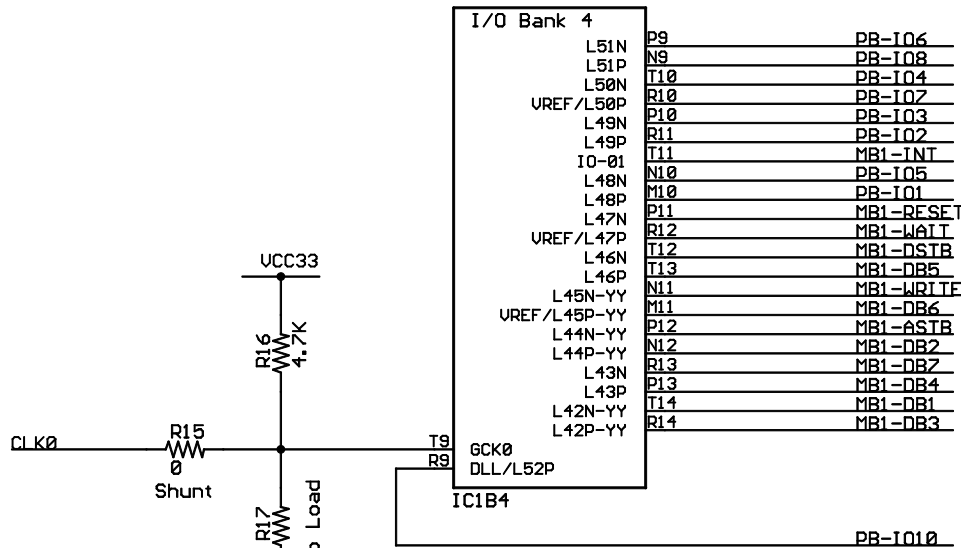
FPGA I/O Banks 0-3



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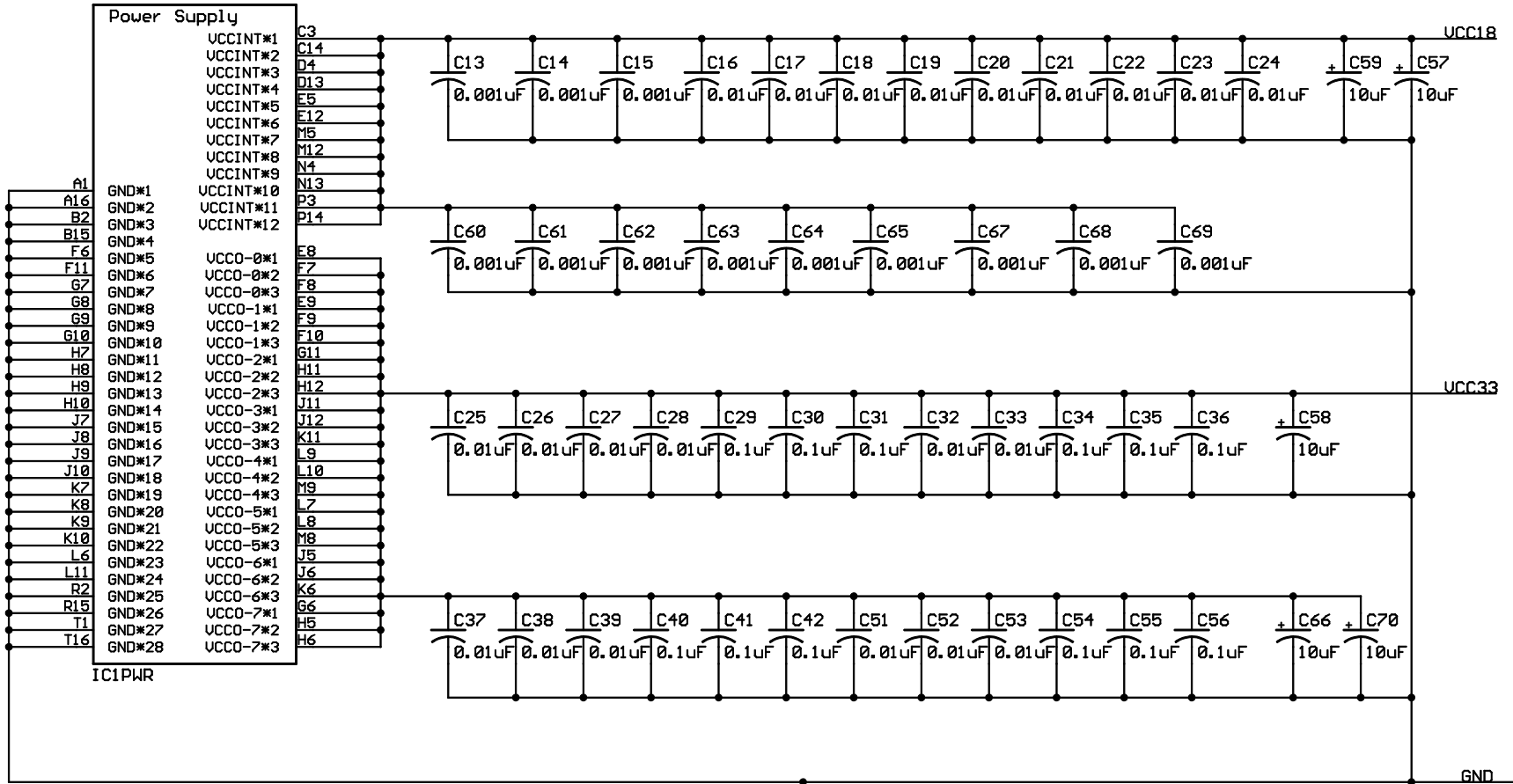
FPGA I/O Banks 4-7



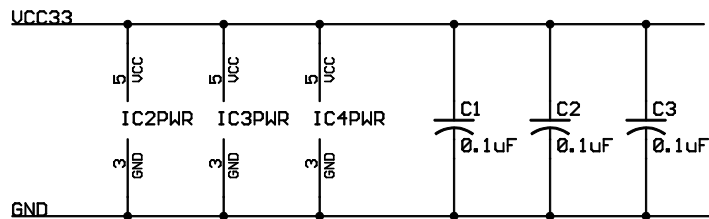
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### FPGA Power Supply and Bypassing

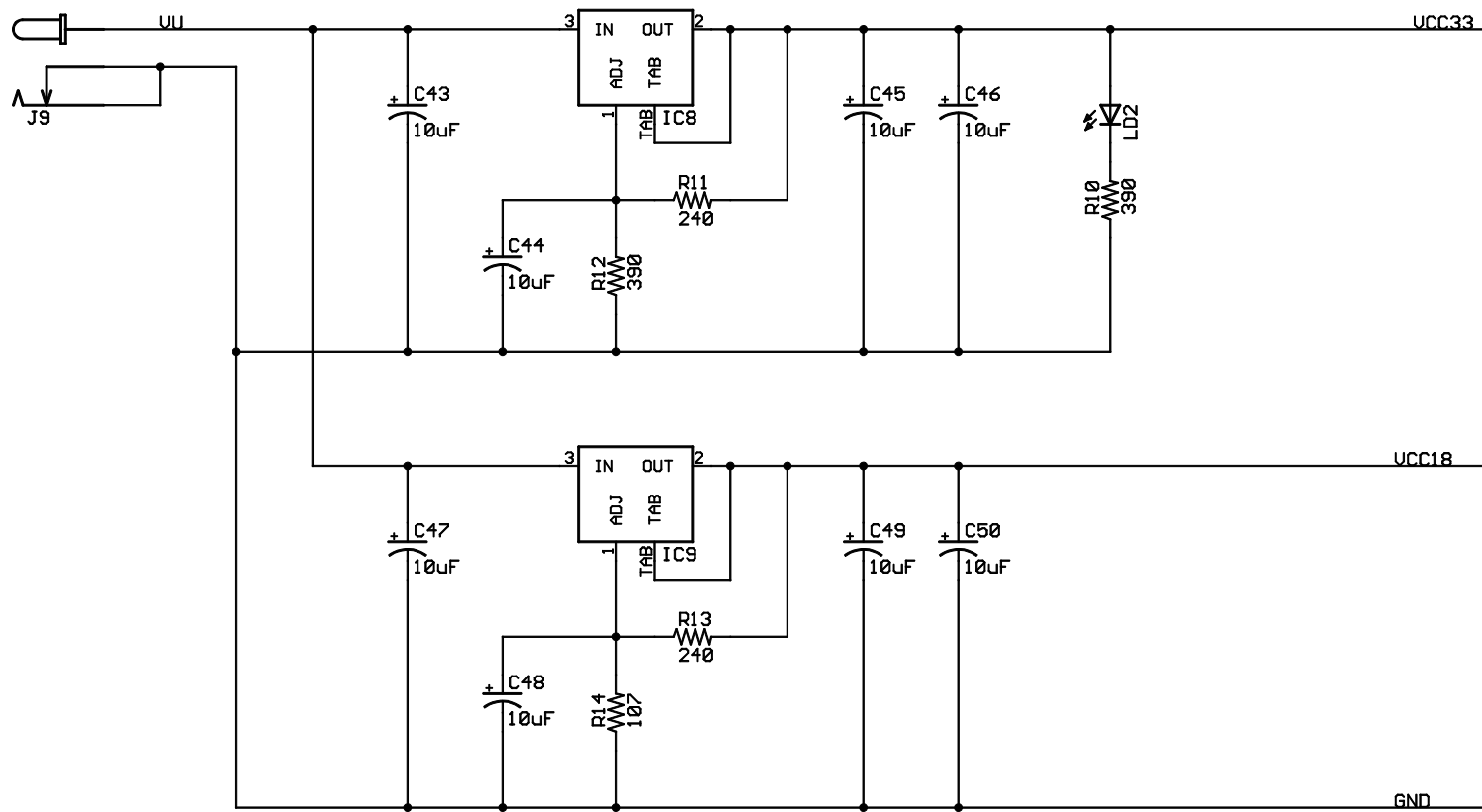


### Misc. Logic Power Supply and Bypassing



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