Virtex-II Electrical Characteristics

Virtex-II devices are provided in –4, –5, and –6 speed grades, with –6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a –4 speed grade industrial device are the same as for a –4 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description(1)		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.0	V
V_{REF}	Input reference voltage	–0.5 to V_{CCO} + 0.5	V
V_{IN} (3)	Input voltage relative to GND (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	–0.5 to 4.0	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temp.	+220	°C
T_J	Operating junction temperature (2)	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging** information on the Xilinx website.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Table 2: **Recommended Operating Conditions**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
	Internal supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.135	3.465	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	3.135	3.465	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.2	3.6	V
V_{BATT}	Battery voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:
1. If battery is not used, do not connect V_{BATT}.
2. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
3. The thresholds for Power On Reset are V_{CCINT} > 1.2V, V_{CCAUX} > 2.5V, and V_{CCO} (Bank 4) > 1.5 V.
4. Limit the noise at the power supply to be within 200 mV peak-to-peak.
5. For power bypassing guidelines, see XAPP623 at www.xilinx.com.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage	All	1.2		V
V_{DRI}	Data retention V_{CCAUX} voltage	All	2.5		V
I_{REF}	V_{REF} current per bank	All	–10	+10	µA
I_L	Input leakage current	All	–10	+10	µA
C_{IN}	Input capacitance	All		10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0 V, V_{CCO} = 3.3 V (sample tested)	All	Note 1	250	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6 V (sample tested)	All	Note 1	250	µA
I_{BATT}	Battery supply current	All		100	nA

Notes:
1. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Min	Typical	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2V40		50	TBD	mA
		XC2V80		50	125	
		XC2V250		65	150	
		XC2V500		80	200	
		XC2V1000		100	250	
		XC2V1500		125	350	
		XC2V2000		150	400	
		XC2V3000		200	500	
		XC2V4000		225	650	
		XC2V6000		250	800	
		XC2V8000		TBD	TBD	
I_{CCOQ}	Quiescent V_{CCO} supply current(1,2)	XC2V40		1	TBD	mA
		XC2V80		1	2	
		XC2V250		1	2	
		XC2V500		1	2	
		XC2V1000		1	2	
		XC2V1500		2	4	
		XC2V2000		2	4	
		XC2V3000		2	4	
		XC2V4000		2	4	
		XC2V6000		2	4	
		XC2V8000		TBD	TBD	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current(1,2)	XC2V40		10	TBD	mA
		XC2V80		10	25	
		XC2V250		10	25	
		XC2V500		10	25	
		XC2V1000		10	25	
		XC2V1500		15	50	
		XC2V2000		15	50	
		XC2V3000		20	75	
		XC2V4000		20	75	
		XC2V6000		25	100	
		XC2V8000		TBD	TBD	

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate values can be obtained by using the Power Estimator or XPOWER™.
3. Data are retained even if V_{CCO} drops to 0 V.
4. Values specified for quiescent supply current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT}, V_{CCAUX}, and V_{CCO} power supplies shall each ramp on no faster than 200 µs and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages.

Table 5 shows the minimum current required by Virtex-II devices for proper power on and configuration.

Power supplies can be turned on in any sequence.

If any V_{CCO} bank powers up before V_{CCAUX}, then each bank draws up to 300 mA, worst case, until the V_{CCAUX} powers on(1). This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Notes:
1. The 300 mA is transient current (peak); it eventually disappears even if V_{CCAUX} does not power up.

Table 5: **Minimum Power On Current Required for Virtex-II Devices**

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	TBD
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	TBD
I_{CCOMIN}	50	50	100	100	100	100	100	TBD

Notes:
1. Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is sessential. Consult Xilinx Application Note 623 for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at www.support.xilinx.com.

V_{CCAUX} can share a power plane with 3.3V V_{CCO}, but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. (More information on SSO is available in Xilinx Answer Record 11713.)

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	16	– 16
LVCMOS15	– 0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	V_{CCO} – 0.4	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.5	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	48	– 8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.6	V_{REF} + 0.6	8	– 8

Table 6: **DC Input and Output Levels *(Continued)***

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.8	V_{REF} + 0.8	16	– 16
SSTL2 I	– 0.5	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.5	V_{REF} – 0.65	V_{REF} + 0.65	7.6	– 7.6
SSTL2 II	– 0.5	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.5	V_{REF} – 0.80	V_{REF} + 0.80	15.2	– 15.2
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTL 12 mA.
2. Tested according to the relevant specifications.
3. LVTTL and LVCMOS inputs have approximately 100 mV of hysteresis.

LDT Differential Signal DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	R_T = 100 Ω across Q and $\overline{Q}$ signals	500	600	700	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	560	600	640	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		500	600	700	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.575	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.925			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential output voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as **Virtex-II Switching Characteristics**, page 9 (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 11: **Pin-to-Pin Performance**

Description	Device Used & Speed Grade	Pin-to-Pin (with I/O delays)	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 –5	6.3	ns
32-bit Address Decoder	XC2V1000 –5	7.7	ns
64-bit Address Decoder	XC2V1000 –5	9.3	ns
4:1 MUX	XC2V1000 –5	5.7	ns
8:1 MUX	XC2V1000 –5	6.5	ns
16:1 MUX	XC2V1000 –5	6.7	ns
32:1 MUX	XC2V1000 –5	8.7	ns
Combinatorial (pad to LUT to pad)	XC2V1000 –5	5.0	ns
Memory			
Block RAM			
Pad to setup		1.6	ns
Clock to Pad		9.5	ns
Distributed RAM			
Pad to setup	XC2V1000 –5	2.7	ns
Clock to Pad	XC2V1000 –5	5.1 (no clk skew)	ns

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

Table 12: **Register-to-Register Performance**

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 –5	398	MHz
32-bit Address Decoder	XC2V1000 –5	291	MHz
64-bit Address Decoder	XC2V1000 –5	274	MHz
4:1 MUX	XC2V1000 –5	563	MHz
8:1 MUX	XC2V1000 –5	454	MHz
16:1 MUX	XC2V1000 –5	414	MHz
32:1 MUX	XC2V1000 –5	323	MHz
Register to LUT to Register	XC2V1000 –5	613	MHz

Table 12: **Register-to-Register Performance *(Continued)***

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
8-bit Adder	XC2V1000 –5	292	MHz
16-bit Adder	XC2V1000 –5	239	MHz
64-bit Adder	XC2V1000 –5	114	MHz
64-bit Counter	XC2V1000 –5	114	MHz
64-bit Accumulator	XC2V1000 –5	110	MHz
Multiplier 18x18 (with Block RAM inputs)	XC2V1000 –5	88	MHz
Multiplier 18x18 (with Register inputs)	XC2V1000 –5	105	MHz
Memory			
Block RAM			
Single-Port 4096 x 4 bits		278	MHz
Single-Port 2048 x 9 bits		277	MHz
Single-Port 1024 x 18 bits		270	MHz
Single-Port 512 x 36 bits		253	MHz
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits		257	MHz
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits		259	MHz
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits		250	MHz
Distributed RAM			
Single-Port 32 x 8-bit	XC2V1000 –5	387	MHz
Single-Port 64 x 8-bit	XC2V1000 –5	335	MHz
Single-Port 128 x 8-bit	XC2V1000 –5	266	MHz
Dual-Port 16 x 8	XC2V1000 –5	409	MHz
Dual-Port 32 x 8	XC2V1000 –5	311	MHz
Dual-Port 64 x 8	XC2V1000 –5	294	MHz
Shift Registers			
128-bit SRL		N/A	MHz
256-bit SRL		N/A	MHz
FIFOs (Async. in Block RAM)			
1024 x 18-bit Read		279	MHz
1024 x 18-bit Write		172	MHz
FIFOs (Sync. in SRL)			
128 x 8-bit		N/A	MHz
128 x 16-bit		N/A	MHz

Virtex-II Switching Characteristics

Switching characteristics in this document are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that **Virtex-II Performance Characteristics**, page 7 are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Virtex-II device with a corresponding speed grade designation.

The values reported in this version of the switching characteristics are extracted from speeds file version 1.111.

Table 13: **Virtex-II Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2V40	–6, –5, –4		
XC2V80	–6		–5, –4
XC2V250	–6		–5, –4
XC2V500	–6		–5, –4
XC2V1000	–6		–5, –4
XC2V1500	–6, –5, –4		
XC2V2000	–6		–5, –4
XC2V3000	–6		–5, –4
XC2V4000	–6		–5, –4
XC2V6000	–6		–5, –4
XC2V8000	–5, –4		

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the Xilinx static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 11.

Table 14: **IOB Input Switching Characteristics**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All	0.69	0.76	0.88	ns, Max
Pad to I output, with delay	T_{IOPID}	XC2V40	1.92	2.11	2.43	ns, Max
		XC2V80	1.92	2.11	2.43	ns, Max
		XC2V250	1.92	2.11	2.43	ns, Max
		XC2V500	1.92	2.11	2.43	ns, Max
		XC2V1000	1.92	2.11	2.43	ns, Max
		XC2V1500	1.92	2.11	2.43	ns, Max
		XC2V2000	1.92	2.11	2.43	ns, Max
		XC2V3000	1.97	2.16	2.49	ns, Max
		XC2V4000	1.97	2.16	2.49	ns, Max
		XC2V6000	2.10	2.31	2.66	ns, Max
		XC2V8000	TBD	TBD	TBD	ns, Max

Table 14: **IOB Input Switching Characteristics *(Continued)***

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.83	0.91	1.05	ns, Max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2V40	3.23	3.55	4.09	ns, Max
		XC2V80	3.23	3.55	4.09	ns, Max
		XC2V250	3.23	3.55	4.09	ns, Max
		XC2V500	3.23	3.55	4.09	ns, Max
		XC2V1000	3.23	3.55	4.09	ns, Max
		XC2V1500	3.23	3.55	4.09	ns, Max
		XC2V2000	3.23	3.55	4.09	ns, Max
		XC2V3000	3.32	3.65	4.20	ns, Max
		XC2V4000	3.32	3.65	4.20	ns, Max
		XC2V6000	3.60	3.95	4.55	ns, Max
		XC2V8000	TBD	TBD	TBD	ns, Max
Clock CLK to output IQ	T_{IOCKIQ}	All	0.61	0.67	0.77	ns, Max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.36	0.92/–0.39	1.06/–0.45	ns, Min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2V40	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V80	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V250	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V2000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V3000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V4000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V6000	3.61/–2.29	3.97/–2.52	4.56/–2.90	ns, Min
		XC2V8000	TBD	TBD	TBD	ns, Min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.19/ 0.03	0.21/ 0.04	0.24/ 0.04	ns, Min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, Min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, Max
GSR to output IQ	T_{GSRQ}	All	7.39	7.99	9.19	ns, Max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

IOB Input Switching Characteristics Standard Adjustments

Table 15: **IOB Input Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0.00	0.00	0.00	ns
	$T_{ILVCMOS33}$	LVCMOS33	0.00	0.00	0.00	ns
	$T_{ILVCMOS25}$	LVCMOS25	0.11	0.11	0.12	ns
	$T_{ILVCMOS18}$	LVCMOS18	0.42	0.43	0.49	ns
	$T_{ILVCMOS15}$	LVCMOS15	0.98	1.00	1.15	ns
	T_{ILVDS_25}	LVDS_25	0.60	0.60	0.69	ns
	T_{ILVDS_33}	LVDS_33	0.60	0.60	0.69	ns
	$T_{ILVPECL\_33}$	LVPECL	0.60	0.60	0.69	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	0.00	0.00	0.00	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	0.00	0.00	0.00	ns
	T_{IPCIX}	PCI–X, 133 MHz, 3.3 V	0.00	0.00	0.00	ns
	T_{IGTL}	GTL	0.42	0.42	0.48	ns
	T_{IGTLP}	GTLP	0.42	0.42	0.48	ns
	T_{IHSTL_I}	HSTL I	0.42	0.42	0.48	ns
	T_{IHSTL_II}	HSTL II	0.42	0.42	0.48	ns
	T_{IHSTL_III}	HSTL III	0.42	0.42	0.48	ns
	T_{IHSTL_IV}	HSTL IV	0.42	0.42	0.48	ns
	$T_{IHSTL\_I\_18}$	HSTL I_18	0.42	0.42	0.48	ns
	$T_{IHSTL\_II\_18}$	HSTL II_18	0.42	0.42	0.48	ns
	$T_{IHSTL\_III\_18}$	HSTL III_18	0.42	0.42	0.48	ns
	$T_{IHSTL\_IV\_18}$	HSTL IV_18	0.42	0.42	0.48	ns
	T_{ISSTL2_I}	SSTL2 I	0.42	0.42	0.48	ns
	T_{ISSTL2_II}	SSTL2 II	0.42	0.42	0.48	ns
	T_{ISSTL3_I}	SSTL3 I	0.35	0.35	0.40	ns
	T_{ISSTL3_II}	SSTL3 II	0.35	0.35	0.40	ns
	T_{IAGP}	AGP	0.35	0.35	0.40	ns
	T_{ILVDCI_33}	LVDCI_33	0.00	0.00	0.00	ns
	T_{ILVDCI_25}	LVDCI_25	0.11	0.11	0.12	ns
	T_{ILVDCI_18}	LVDCI_18	0.42	0.43	0.49	ns

Table 15: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{ILVDCI_15}	LVDCI_15	0.98	1.00	1.14	ns
	$T_{ILVDCI\_DV2\_33}$	LVDCI_DV2_33	0.00	0.00	0.00	ns
	$T_{ILVDCI\_DV2\_25}$	LVDCI_DV2_25	0.11	0.11	0.12	ns
	$T_{ILVDCI\_DV2\_18}$	LVDCI_DV2_18	0.42	0.43	0.49	ns
	$T_{ILVDCI\_DV2\_15}$	LVDCI_DV2_15	0.98	1.00	1.14	ns
	T_{IGTL_DCI}	GTL_DCI	0.42	0.42	0.48	ns
	T_{IGTLP_DCI}	GTLP_DCI	0.42	0.42	0.48	ns
	$T_{IHSTL\_I\_DCI}$	HSTL_I_DCI	0.42	0.42	0.48	ns
	$T_{IHSTL\_II\_DCI}$	HSTL_II_DCI	0.42	0.42	0.48	ns
	$T_{IHSTL\_III\_DCI}$	HSTL_III_DCI	0.42	0.42	0.48	ns
	$T_{IHSTL\_IV\_DCI}$	HSTL_IV_DCI	0.42	0.42	0.48	ns
	$T_{IHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18	0.42	0.42	0.48	ns
	$T_{IHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18	0.42	0.42	0.48	ns
	$T_{IHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18	0.42	0.42	0.48	ns
	$T_{IHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18	0.42	0.42	0.48	ns
	$T_{ISSTL2\_I\_DCI}$	SSTL2_I_DCI	0.42	0.42	0.48	ns
	$T_{ISSTL2\_II\_DCI}$	SSTL2_II_DCI	0.42	0.42	0.48	ns
	$T_{ISSTL3\_I\_DCI}$	SSTL3_I_DCI	0.35	0.35	0.40	ns
	$T_{ISSTL3\_II\_DCI}$	SSTL3_II_DCI	0.35	0.35	0.40	ns
	T_{ILDT_25}	LDT_25	0.48	0.49	0.56	ns
	T_{IULVDS_25}	ULVDS_25	0.48	0.49	0.56	ns

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 14.

Table 16: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–6**	**–5**	**–4**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	2.52	2.63	3.03	ns, Max
O input to Pad via transparent latch	T_{IOOLP}	2.81	2.95	3.40	ns, Max
3-State Delays					
T input to Pad high-impedance(1)	T_{IOTHZ}	0.51	0.56	0.64	ns, Max
T input to valid data on Pad	T_{IOTON}	2.47	2.57	2.96	ns, Max
T input to Pad high-impedance via transparent latch(1)	$T_{IOTLPHZ}$	0.80	0.88	1.01	ns, Max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	2.76	2.89	3.33	ns, Max
GTS to Pad high impedance(1)	T_{GTS}	6.69	7.22	8.30	ns, Max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	2.84	2.99	3.44	ns, Max
Clock CLK to Pad high-impedance (synchronous)(1)	T_{IOCKHZ}	0.95	1.04	1.20	ns, Max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	2.90	3.06	3.51	ns, Max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.31/–0.08	0.34/–0.09	0.39/–0.11	ns, Min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, Min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.28/–0.06	0.31/–0.07	0.35/–0.08	ns, Min
3–State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
3–State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, Min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}	3.50	3.71	4.26	ns, Max
SR input to Pad high-impedance (asynchronous)(1)	T_{IOSRHZ}	1.52	1.67	1.92	ns, Max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	3.47	3.68	4.23	ns, Max
GSR to Pad	T_{IOGSRQ}	5.44	5.98	6.88	ns, Max

Notes:
1. The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: **IOB Output Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	15.28	15.73	18.09	ns
	T_{OLVTTL_S4}	4 mA	8.61	8.87	10.20	ns
	T_{OLVTTL_S6}	6 mA	5.94	6.11	7.03	ns
	T_{OLVTTL_S8}	8 mA	3.68	3.79	4.35	ns
	T_{OLVTTL_S12}	12 mA	2.61	2.69	3.09	ns
	T_{OLVTTL_S16}	16 mA	1.65	1.70	1.96	ns
	T_{OLVTTL_S24}	24 mA	1.08	1.11	1.28	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA	12.16	12.52	14.40	ns
	T_{OLVTTL_F4}	4 mA	5.09	5.25	6.03	ns
	T_{OLVTTL_F6}	6 mA	3.26	3.35	3.85	ns
	T_{OLVTTL_F8}	8 mA	0.53	0.54	0.62	ns
	T_{OLVTTL_F12}	12 mA	0.00	0.00	0.00	ns
	T_{OLVTTL_F16}	16 mA	–0.43	–0.45	–0.51	ns
	T_{OLVTTL_F24}	24 mA	–0.60	–0.62	–0.71	ns
	T_{OLVDS_25}	LVDS	–1.27	–1.31	–1.51	ns
	T_{OLVDS_33}	LVDS	–1.07	–1.11	–1.27	ns
	$T_{OLVDSEXT\_25}$	LVDS	–1.15	–1.19	–1.37	ns
	$T_{OLVDSEXT\_33}$	LVDS	–1.14	–1.18	–1.35	ns
	T_{OLDT_25}	LDT	–1.21	–1.25	–1.44	ns
	T_{OBLVDS_25}	BLVDS	0.67	0.69	0.79	ns
	T_{OULVDS_25}	ULVDS	–1.21	–1.25	–1.44	ns
	$T_{OLVPECL\_33}$	LVPECL	0.14	0.15	0.17	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	–0.22	–0.22	–0.26	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	–0.85	–0.88	–1.01	ns
	T_{OPCIX}	PCI–X, 133 MHz, 3.3 V	–0.84	–0.87	–1.00	ns
	T_{OGTL}	GTL	–1.31	–1.35	–1.55	ns
	T_{OGTLP}	GTLP	–1.05	–1.09	–1.25	ns
	T_{OHSTL_I}	HSTL I	–0.65	–0.67	–0.77	ns
	T_{OHSTL_II}	HSTL II	–1.04	–1.07	–1.24	ns
	T_{OHSTL_III}	HSTL III	–1.06	–1.09	–1.26	ns
	T_{OHSTL_IV}	HSTL IV	–1.28	–1.32	–1.51	ns
	$T_{OHSTL\_I\_18}$	HSTL I_18	–0.83	–0.85	–0.98	ns
	$T_{OHSTL\_II\_18}$	HSTL II_18	–1.07	–1.10	–1.27	ns
	$T_{OHSTL\_III\_18}$	HSTL III_18	–1.05	–1.08	–1.24	ns
	$T_{OHSTL\_IV\_18}$	HSTL IV_18	–1.26	–1.29	–1.49	ns

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{OSSTL2_I}	SSTL2 I	–0.73	–0.75	–0.87	ns
	T_{OSSTL2_II}	SSTL2 II	–1.10	–1.13	–1.30	ns
	T_{OSSTL3_I}	SSTL3 I	–0.65	–0.67	–0.78	ns
	T_{OSSTL3_II}	SSTL3 II	–1.01	–1.04	–1.20	ns
	T_{OAGP}	AGP	–1.07	–1.10	–1.27	ns
	$T_{OLVCMOS33\_S2}$	LVCMOS33, Slow, 2 mA	13.63	14.04	16.14	ns
	$T_{OLVCMOS33\_S4}$	4 mA	6.45	6.64	7.63	ns
	$T_{OLVCMOS33\_S6}$	6 mA	4.56	4.70	5.40	ns
	$T_{OLVCMOS33\_S8}$	8 mA	2.62	2.70	3.11	ns
	$T_{OLVCMOS33\_S12}$	12 mA	1.87	1.93	2.21	ns
	$T_{OLVCMOS33\_S16}$	16 mA	1.15	1.18	1.36	ns
	$T_{OLVCMOS33\_S24}$	24 mA	0.91	0.94	1.08	ns
	$T_{OLVCMOS33\_F2}$	LVCMOS33, Fast, 2 mA	11.63	11.97	13.77	ns
	$T_{OLVCMOS33\_F4}$	4 mA	4.64	4.78	5.49	ns
	$T_{OLVCMOS33\_F6}$	6 mA	2.14	2.20	2.53	ns
	$T_{OLVCMOS33\_F8}$	8 mA	0.48	0.50	0.57	ns
	$T_{OLVCMOS33\_F12}$	12 mA	0.04	0.05	0.05	ns
	$T_{OLVCMOS33\_F16}$	16 mA	–0.48	–0.49	–0.57	ns
	$T_{OLVCMOS33\_F24}$	24 mA	–0.58	–0.60	–0.69	ns
	$T_{OLVCMOS25\_S2}$	LVCMOS25, Slow, 2 mA	12.68	13.05	15.01	ns
	$T_{OLVCMOS25\_S4}$	4 mA	6.57	6.76	7.78	ns
	$T_{OLVCMOS25\_S6}$	6 mA	5.83	6.00	6.90	ns
	$T_{OLVCMOS25\_S8}$	8 mA	4.84	4.98	5.73	ns
	$T_{OLVCMOS25\_S12}$	12 mA	3.03	3.12	3.59	ns
	$T_{OLVCMOS25\_S16}$	16 mA	2.33	2.40	2.76	ns
	$T_{OLVCMOS25\_S24}$	24 mA	1.83	1.89	2.17	ns
	$T_{OLVCMOS25\_F2}$	LVCMOS25, Fast, 2 mA	9.05	9.32	10.72	ns
	$T_{OLVCMOS25\_F4}$	4 mA	3.45	3.55	4.09	ns
	$T_{OLVCMOS25\_F6}$	6 mA	1.11	1.14	1.31	ns
	$T_{OLVCMOS25\_F8}$	8 mA	0.49	0.51	0.58	ns
	$T_{OLVCMOS25\_F12}$	12 mA	–0.11	–0.11	–0.13	ns
	$T_{OLVCMOS25\_F16}$	16 mA	–0.37	–0.38	–0.44	ns
	$T_{OLVCMOS25\_F24}$	24 mA	–0.61	–0.63	–0.72	ns
	$T_{OLVCMOS18\_S2}$	LVCMOS18, Slow, 2 mA	20.74	21.36	24.57	ns
	$T_{OLVCMOS18\_S4}$	4 mA	12.35	12.72	14.63	ns
	$T_{OLVCMOS18\_S6}$	6 mA	8.76	9.02	10.37	ns
	$T_{OLVCMOS18\_S8}$	8 mA	7.84	8.08	9.29	ns
	$T_{OLVCMOS18\_S12}$	12 mA	5.85	6.03	6.93	ns
	$T_{OLVCMOS18\_S16}$	16 mA	5.46	5.62	6.46	ns
	$T_{OLVCMOS18\_F2}$	LVCMOS18, Fast, 2 mA	9.63	9.92	11.40	ns

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	$T_{OLVCMOS18\_F4}$	4 mA	4.29	4.41	5.08	ns
	$T_{OLVCMOS18\_F6}$	6 mA	1.61	1.66	1.91	ns
	$T_{OLVCMOS18\_F8}$	8 mA	1.03	1.06	1.22	ns
	$T_{OLVCMOS18\_F12}$	12 mA	0.26	0.27	0.31	ns
	$T_{OLVCMOS18\_F16}$	16 mA	0.11	0.11	0.12	ns
	$T_{OLVCMOS15\_S2}$	LVCMOS15, Slow, 2 mA	23.54	24.25	27.88	ns
	$T_{OLVCMOS15\_S4}$	4 mA	14.89	15.34	17.64	ns
	$T_{OLVCMOS15\_S6}$	6 mA	13.58	13.99	16.08	ns
	$T_{OLVCMOS15\_S8}$	8 mA	10.62	10.94	12.58	ns
	$T_{OLVCMOS15\_S12}$	12 mA	9.58	9.86	11.34	ns
	$T_{OLVCMOS15\_S16}$	16 mA	8.65	8.91	10.24	ns
	$T_{OLVCMOS15\_F2}$	LVCMOS15, Fast, 2 mA	9.13	9.40	10.81	ns
	$T_{OLVCMOS15\_F4}$	4 mA	4.84	4.99	5.74	ns
	$T_{OLVCMOS15\_F6}$	6 mA	2.20	2.27	2.61	ns
	$T_{OLVCMOS15\_F8}$	8 mA	1.16	1.20	1.38	ns
	$T_{OLVCMOS15\_F12}$	12 mA	0.75	0.78	0.89	ns
	$T_{OLVCMOS15\_F16}$	16 mA	0.61	0.63	0.72	ns
	T_{OLVDCI_33}	LVDCI_33	1.91	1.97	2.26	ns
	T_{OLVDCI_25}	LVDCI_25	1.36	1.40	1.61	ns
	T_{OLVDCI_18}	LVDCI_18	1.29	1.33	1.53	ns
	T_{OLVDCI_15}	LVDCI_15	0.96	0.99	1.14	ns
	$T_{OLVDCI\_DV2\_33}$	LVDCI_DV2_33	1.91	1.97	2.27	ns
	$T_{OLVDCI\_DV2\_25}$	LVDCI_DV2_25	1.36	1.40	1.61	ns
	$T_{OLVDCI\_DV2\_18}$	LVDCI_DV2_18	1.03	1.06	1.22	ns
	$T_{OLVDCI\_DV2\_15}$	LVDCI_DV2_15	0.94	0.96	1.11	ns
	T_{OGTL_DCI}	GTL_DCI	–1.38	–1.42	–1.63	ns
	T_{OGTLP_DCI}	GTLP_DCI	–1.00	–1.03	–1.18	ns
	$T_{OHSTL\_I\_DCI}$	HSTL_I_DCI	–0.65	–0.67	–0.77	ns
	$T_{OHSTL\_II\_DCI}$	HSTL_II_DCI	–0.72	–0.74	–0.85	ns
	$T_{OHSTL\_III\_DCI}$	HSTL_III_DCI	–1.09	–1.12	–1.29	ns
	$T_{OHSTL\_IV\_DCI}$	HSTL_IV_DCI	–1.35	–1.39	–1.59	ns
	$T_{OHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18	–0.84	–0.86	–0.99	ns
	$T_{OHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18	–0.94	–0.97	–1.12	ns
	$T_{OHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18	–1.05	–1.08	–1.24	ns
	$T_{OHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18	–1.28	–1.32	–1.52	ns
	$T_{OSSTL2\_I\_DCI}$	SSTL2_I_DCI	–0.84	–0.86	–0.99	ns
	$T_{OSSTL2\_II\_DCI}$	SSTL2_II_DCI	–1.02	–1.05	–1.20	ns
	$T_{OSSTL3\_I\_DCI}$	SSTL3_I_DCI	–0.85	–0.88	–1.01	ns
	$T_{OSSTL3\_II\_DCI}$	SSTL3_II_DCI	–0.74	–0.76	–0.88	ns

Table 18: **Delay Measurement Methodology**

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	–
LVCMOS33	0	3.3	1.65	–
LVCMOS25	0	2.5	1.25	–
LVCMOS18	0	1.8	0.9	–
LVCMOS15	0	1.5	0.75	–
PCI33_3	Per PCI Specification			–
PCI66_3	Per PCI Specification			–
PCIX33_3	Per PCI–X Specification			–
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL	1.6 –0.3	1.6 + 0.3	1.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

Table 19: **Standard Capacitive Loads**

Standard	Csl (pF)
LVTTL Fast Slew Rate, 2mA drive	35
LVTTL Fast Slew Rate, 4mA drive	35
LVTTL Fast Slew Rate, 6mA drive	35
LVTTL Fast Slew Rate, 8mA drive	35
LVTTL Fast Slew Rate, 12mA drive	35
LVTTL Fast Slew Rate, 16mA drive	35
LVTTL Fast Slew Rate, 24mA drive	35
LVTTL Slow Slew Rate, 2mA drive	35
LVTTL Slow Slew Rate, 4mA drive	35
LVTTL Slow Slew Rate, 6mA drive	35
LVTTL Slow Slew Rate, 8mA drive	35
LVTTL Slow Slew Rate, 12mA drive	35
LVTTL Slow Slew Rate, 16mA drive	35
LVTTL Slow Slew Rate, 24mA drive	35
LVCMOS33	35
LVCMOS25	35
LVCMOS18	35
LVCMOS15	35
PCI 33MHZ 3.3 V	10
PCI 66 MHz 3.3 V	10
PCI–X 133 MHz 3.3 V	10
GTL	0
GTLP	0
HSTL Class I	10
HSTL Class II	10
HSTL Class III	10
HSTL Class IV	10
SSTL2 Class I	10
SSTL2 Class II	10
SSTL3 Class I	10
SSTL3 Class II	10
AGP	10

Notes:
1. I/O parameter measurements are made with the capacitance values shown above.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.
3. Use of IBIS models results in a more accurate prediction of the propagation delay:
   a. Model the output in an IBIS simulation into the standard capacitive load.
   b. Record the relative time to the V_{OH} or V_{OL} transition of interest.
   c. Remove the capacitance, and model the actual PCB traces (transmission lines) and actual loads from the appropriate IBIS models for driven devices.
   d. Record the results from the new simulation.
   e. Compare with the capacitance simulation. The increase or decrease in delay from the capacitive load delay simulation should be added or subtracted from the value above to predict the actual delay.

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

CLB Distributed RAM Switching Characteristics

Table 22: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.63	1.79	2.05	ns, Max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.97	2.17	2.49	ns, Max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.77	1.94	2.23	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.53/–0.09	0.58/–0.10	0.67/–0.11	ns, Min
F/G address inputs	T_{AS}/T_{AH}	0.40/ 0.00	0.44/ 0.00	0.50/ 0.00	ns, Min
SR input (WS)	T_{WES}/T_{WEH}	0.42/–0.01	0.46/–0.01	0.53/–0.01	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{WPL}	0.57	0.63	0.72	ns, Min
Minimum clock period to meet address write cycle time	T_{WC}	1.14	1.25	1.44	ns, Min

CLB Shift Register Switching Characteristics

Table 23: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.31	2.54	2.92	ns, Max
Clock CLK to X/Y outputs	T_{REG32}	2.65	2.92	3.35	ns, Max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.23	2.46	2.82	ns, Max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.18	2.40	2.75	ns, Max
Clock CLK to Shiftout	T_{CKSH}	1.92	2.11	2.43	ns, Max
Clock CLK to F5 output	T_{REGF5}	2.45	2.69	3.09	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.53/–0.07	0.58/–0.08	0.67/–0.09	ns, Min
SR input (WS)	T_{WSS}/T_{WSH}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{SRPL}	0.57	0.63	0.72	ns, Min

Multiplier Switching Characteristics

Table 24: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

Table 25: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T_{MULTCK_P35}	2.76	6.91	8.12	ns, Max
Clock to Pin 34	T_{MULTCK_P34}	2.66	6.75	7.93	ns, Max
Clock to Pin 33	T_{MULTCK_P33}	2.56	6.59	7.74	ns, Max
Clock to Pin 32	T_{MULTCK_P32}	2.47	6.43	7.56	ns, Max
Clock to Pin 31	T_{MULTCK_P31}	2.37	6.27	7.37	ns, Max
Clock to Pin 30	T_{MULTCK_P30}	2.27	6.11	7.19	ns, Max
Clock to Pin 29	T_{MULTCK_P29}	2.17	5.95	7.00	ns, Max
Clock to Pin 28	T_{MULTCK_P28}	2.08	5.79	6.81	ns, Max
Clock to Pin 27	T_{MULTCK_P27}	1.98	5.63	6.63	ns, Max
Clock to Pin 26	T_{MULTCK_P26}	1.88	5.47	6.44	ns, Max
Clock to Pin 25	T_{MULTCK_P25}	1.79	5.31	6.26	ns, Max
Clock to Pin 24	T_{MULTCK_P24}	1.69	5.15	6.07	ns, Max
Clock to Pin 23	T_{MULTCK_P23}	1.59	4.99	5.88	ns, Max
Clock to Pin 22	T_{MULTCK_P22}	1.50	4.83	5.70	ns, Max
Clock to Pin 21	T_{MULTCK_P21}	1.40	4.67	5.51	ns, Max
Clock to Pin 20	T_{MULTCK_P20}	1.30	4.51	5.33	ns, Max
Clock to Pin 19	T_{MULTCK_P19}	1.20	4.35	5.14	ns, Max
Clock to Pin 18	T_{MULTCK_P18}	1.11	4.19	4.95	ns, Max
Clock to Pin 17	T_{MULTCK_P17}	1.01	4.03	4.77	ns, Max
Clock to Pin 16	T_{MULTCK_P16}	0.91	3.87	4.58	ns, Max
Clock to Pin 15	T_{MULTCK_P15}	0.91	3.71	4.40	ns, Max
Clock to Pin 14	T_{MULTCK_P14}	0.91	3.55	4.21	ns, Max
Clock to Pin 13	T_{MULTCK_P13}	0.91	3.39	4.02	ns, Max
Clock to Pin 12	T_{MULTCK_P12}	0.91	3.23	3.84	ns, Max
Clock to Pin 11	T_{MULTCK_P11}	0.91	3.07	3.65	ns, Max
Clock to Pin 10	T_{MULTCK_P10}	0.91	2.91	3.47	ns, Max
Clock to Pin 9	T_{MULTCK_P9}	0.91	2.75	3.28	ns, Max
Clock to Pin 8	T_{MULTCK_P8}	0.91	2.59	3.09	ns, Max
Clock to Pin 7	T_{MULTCK_P7}	0.91	2.43	2.91	ns, Max
Clock to Pin 6	T_{MULTCK_P6}	0.91	2.27	2.72	ns, Max
Clock to Pin 5	T_{MULTCK_P5}	0.91	2.11	2.54	ns, Max
Clock to Pin 4	T_{MULTCK_P4}	0.91	1.95	2.35	ns, Max
Clock to Pin 3	T_{MULTCK_P3}	0.91	1.79	2.16	ns, Max
Clock to Pin 2	T_{MULTCK_P2}	0.91	1.63	1.98	ns, Max
Clock to Pin 1	T_{MULTCK_P1}	0.91	1.47	1.79	ns, Max
Clock to Pin 0	T_{MULTCK_P0}	0.91	1.31	1.61	ns, Max

Enhanced Multiplier Switching Characteristics

Table 26 and Table 27 provide timing information for enhanced Virtex-II multiplier blocks, available in stepping revisions of Virtex-II devices. For more information on stepping revisions, availability, and ordering instructions, see your local sales representative.

Table 26: **Enhanced Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	5.14	5.91	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	5.03	5.79	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	4.93	5.66	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	4.82	5.54	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	4.71	5.42	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	4.61	5.29	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	4.50	5.17	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	4.39	5.05	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	4.28	4.92	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	4.18	4.80	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	4.07	4.68	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	3.96	4.56	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	3.86	4.43	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	3.75	4.31	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	3.64	4.19	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	3.54	4.06	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	3.43	3.94	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	3.32	3.82	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	3.21	3.69	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	3.11	3.57	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	3.00	3.45	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	2.89	3.33	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	2.79	3.20	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	2.68	3.08	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	2.57	2.96	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	2.47	2.83	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	2.36	2.71	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	2.25	2.59	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	2.14	2.46	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	2.04	2.34	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	1.93	2.22	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	1.82	2.10	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	1.72	1.97	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	1.61	1.85	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	1.50	1.73	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	1.40	1.60	ns, Max

Table 27: **Enhanced Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T_{MULTCK_P35}	2.95	3.25	3.74	ns, Max
Clock to Pin 34	T_{MULTCK_P34}	2.85	3.14	3.61	ns, Max
Clock to Pin 33	T_{MULTCK_P33}	2.76	3.04	3.49	ns, Max
Clock to Pin 32	T_{MULTCK_P32}	2.66	2.93	3.37	ns, Max
Clock to Pin 31	T_{MULTCK_P31}	2.56	2.82	3.25	ns, Max
Clock to Pin 30	T_{MULTCK_P30}	2.47	2.72	3.12	ns, Max
Clock to Pin 29	T_{MULTCK_P29}	2.37	2.61	3.00	ns, Max
Clock to Pin 28	T_{MULTCK_P28}	2.27	2.50	2.88	ns, Max
Clock to Pin 27	T_{MULTCK_P27}	2.17	2.40	2.75	ns, Max
Clock to Pin 26	T_{MULTCK_P26}	2.08	2.29	2.63	ns, Max
Clock to Pin 25	T_{MULTCK_P25}	1.98	2.18	2.51	ns, Max
Clock to Pin 24	T_{MULTCK_P24}	1.88	2.07	2.38	ns, Max
Clock to Pin 23	T_{MULTCK_P23}	1.79	1.97	2.26	ns, Max
Clock to Pin 22	T_{MULTCK_P22}	1.69	1.86	2.14	ns, Max
Clock to Pin 21	T_{MULTCK_P21}	1.59	1.75	2.02	ns, Max
Clock to Pin 20	T_{MULTCK_P20}	1.50	1.65	1.89	ns, Max
Clock to Pin 19	T_{MULTCK_P19}	1.40	1.54	1.77	ns, Max
Clock to Pin 18	T_{MULTCK_P18}	1.30	1.43	1.65	ns, Max
Clock to Pin 17	T_{MULTCK_P17}	1.20	1.33	1.52	ns, Max
Clock to Pin 16	T_{MULTCK_P16}	1.11	1.22	1.40	ns, Max
Clock to Pin 15	T_{MULTCK_P15}	1.01	1.11	1.28	ns, Max
Clock to Pin 14	T_{MULTCK_P14}	0.91	1.00	1.15	ns, Max
Clock to Pin 13	T_{MULTCK_P13}	0.91	1.00	1.15	ns, Max
Clock to Pin 12	T_{MULTCK_P12}	0.91	1.00	1.15	ns, Max
Clock to Pin 11	T_{MULTCK_P11}	0.91	1.00	1.15	ns, Max
Clock to Pin 10	T_{MULTCK_P10}	0.91	1.00	1.15	ns, Max
Clock to Pin 9	T_{MULTCK_P9}	0.91	1.00	1.15	ns, Max
Clock to Pin 8	T_{MULTCK_P8}	0.91	1.00	1.15	ns, Max
Clock to Pin 7	T_{MULTCK_P7}	0.91	1.00	1.15	ns, Max
Clock to Pin 6	T_{MULTCK_P6}	0.91	1.00	1.15	ns, Max
Clock to Pin 5	T_{MULTCK_P5}	0.91	1.00	1.15	ns, Max
Clock to Pin 4	T_{MULTCK_P4}	0.91	1.00	1.15	ns, Max
Clock to Pin 3	T_{MULTCK_P3}	0.91	1.00	1.15	ns, Max
Clock to Pin 2	T_{MULTCK_P2}	0.91	1.00	1.15	ns, Max
Clock to Pin 1	T_{MULTCK_P1}	0.91	1.00	1.15	ns, Max
Clock to Pin 0	T_{MULTCK_P0}	0.91	1.00	1.15	ns, Max

Block SelectRAM Switching Characteristics

Table 28: **Block SelectRAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	2.10	2.31	2.65	ns, Max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, Min
DIN inputs	T_{BDCK}/T_{BCKD}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, Min
EN input	T_{BECK}/T_{BCKE}	0.95/–0.46	1.04/–0.50	1.20/–0.58	ns, Min
RST input	T_{BRCK}/T_{BCKR}	1.31/–0.71	1.44/–0.78	1.65/–0.90	ns, Min
WEN input	T_{BWCK}/T_{BCKW}	0.57/–0.19	0.63/–0.21	0.72/–0.25	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}	1.17	1.29	1.48	ns, Min
Minimum Pulse Width, Low	T_{BPWL}	1.17	1.29	1.48	ns, Min

TBUF Switching Characteristics

Table 29: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
IN input to OUT output	T_{IO}	0.45	0.50	0.58	ns, Max
TRI input to OUT output high-impedance	T_{OFF}	0.44	0.48	0.55	ns, Max
TRI input to valid data on OUT output	T_{ON}	0.44	0.48	0.55	ns, Max

JTAG Test Access Port Switching Characteristics

Table 30: **JTAG Test Access Port Switching Characteristics**

Description	Symbol		Units
TMS and TDI Setup times before TCK	T_{TAPTK}	5.5	ns, Min
TMS and TDI Hold times after TCK	T_{TCKTAP}	0.0	ns, Min
Output delay from clock TCK to output TDO	T_{TCKTDO}	10.0	ns, Max
Maximum TCK clock frequency	F_{TCK}	33	MHz, Max

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM

Table 31: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output delay using Output flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 14.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2V40	2.19	2.40	2.76	ns
		XC2V80	2.19	2.40	2.76	ns
		XC2V250	2.19	2.40	2.76	ns
		XC2V500	2.19	2.40	2.76	ns
		XC2V1000	2.19	2.40	2.76	ns
		XC2V1500	2.19	2.40	2.76	ns
		XC2V2000	2.19	2.40	2.76	ns
		XC2V3000	2.28	2.50	2.88	ns
		XC2V4000	2.28	2.50	2.88	ns
		XC2V6000	2.73	3.00	3.45	ns
		XC2V8000	TBD	TBD	TBD	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured with a 35 pF external capacitive load. The only time it is not 50% of V_{CC} threshold is with LVCMOS. For other I/O standards and different loads, see Table 18.
3. DCM output jitter is included in the measurement.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 32: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 14.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2V40	4.28	4.70	4.98	ns
		XC2V80	4.28	4.70	4.98	ns
		XC2V250	4.50	5.00	5.75	ns
		XC2V500	4.50	5.00	5.75	ns
		XC2V1000	5.10	5.40	5.90	ns
		XC2V1500	5.10	5.40	5.90	ns
		XC2V2000	5.20	5.55	6.38	ns
		XC2V3000	5.23	5.76	6.62	ns
		XC2V4000	5.55	6.11	7.02	ns
		XC2V6000	6.00	6.50	7.22	ns
		XC2V8000	TBD	TBD	TBD	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 18.

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTL Standard, *With* DCM

Table 33: **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2V40	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V80	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V250	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1000	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V2000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V3000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V4000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V6000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V8000	TBD	TBD	TBD	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DCM output jitter is included in the measurement.

Global Clock Setup and Hold for LVTTL Standard, *Without* DCM

Table 34: **Global Clock Setup and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.(2) For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 11.						
Full Delay Global Clock and IFF(1) without DCM	T_{PSFD}/T_{PHFD}	XC2V40	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V80	2.10/ 0.00	2.10/ 0.00	2.21/ 0.00	ns
		XC2V250	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V1500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V2000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V3000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		XC2V4000	2.00/ 0.00	2.00/ 0.00	2.30/ 0.00	ns
		XC2V6000	1.92/ 0.50	1.92/ 0.50	2.21/ 0.50	ns
		XC2V8000	TBD	TBD	TBD	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. These values are parametrically measured.

DCM Timing Parameters

All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 35: **Operating Frequency Ranges**

Description	Symbol	Constraints	Speed Grade			Units
			–6	–5	–4	
Output Clocks (Low Frequency Mode)						
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_1X_LF_Max		230.00	210.00	180.00	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_2X_LF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_LF_Min		1.50	1.50	1.50	MHz
	CLKOUT_FREQ_DV_LF_Max		150.00	140.00	120.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs) (1), (3)	CLKIN_FREQ_DLL_LF_Min		24.00	24.00	24.00	MHz
	CLKIN_FREQ_DLL_LF_Max		230.00	210.00	180.00	MHz
CLKIN (using CLKFX outputs) (2), (3)	CLKIN_FREQ_FX_LF_Min		1.00	1.00	1.00	MHz
	CLKIN_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
PSCLK	PSCLK_FREQ_LF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_LF_Max		450.00	420.00	360.00	MHz
Output Clocks (High Frequency Mode)						
CLK0, CLK180	CLKOUT_FREQ_1X_HF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_1X_HF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_HF_Min		3.00	3.00	3.00	MHz
	CLKOUT_FREQ_DV_HF_Max		300.00	280.00	240.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_Min		210.00	210.00	210.00	MHz
	CLKOUT_FREQ_FX_HF_Max		350.00	320.00	270.00	MHz
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs) (1), (3)	CLKIN_FREQ_DLL_HF_Min		48.00	48.00	48.00	MHz
	CLKIN_FREQ_DLL_HF_Max		450.00	420.00	360.00	MHz
CLKIN (using CLKFX outputs) (2), (3)	CLKIN_FRQ_FX_HF_Min		50.00	50.00	50.00	MHz
	CLKIN_FRQ_FX_HF_Max		350.00	320.00	270.00	MHz
PSCLK	PSCLK_FREQ_HF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_HF_Max		450.00	420.00	360.00	MHz

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used, then double these values.

Input Clock Tolerances

Table 36: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/high Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(2)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. ""DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.

Output Clock Jitter

Table 37: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			–6	–5	–4	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0		±100	±100	±100	ps
CLK90	CLKOUT_PER_JITT_90		±150	±150	±150	ps
CLK180	CLKOUT_PER_JITT_180		±150	±150	±150	ps
CLK270	CLKOUT_PER_JITT_270		±150	±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X		±200	±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1		±150	±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2		±300	±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX		Note 1	Note 1	Note 1	ps

Notes:
1. Values for this parameter are available at www.xilinx.com.

Output Clock Phase Alignment

Table 38: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			–6	–5	–4	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE		±50	±50	±50	ps
Phase Offset Between Any DCM Outputs						
All CLK* outputs	CLKOUT_PHASE		±140	±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(2)		±150	±150	±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX		±100	±100	±100	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

Miscellaneous Timing Parameters

Table 39: **Miscellaneous Timing Parameters**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade			Units
			–6	–5	–4	
Time Required to Achieve LOCK						
Using DLL outputs(1)	LOCK_DLL					
	LOCK_DLL_60	> 60MHz	20.0	20.0	20.0	µs
	LOCK_DLL_50_60	50 - 60 MHz	25.0	25.0	25.0	µs
	LOCK_DLL_40_50	40 - 50 MHz	50.0	50.0	50.0	µs
	LOCK_DLL_30_40	30 - 40 MHz	90.0	90.0	90.0	µs
	LOCK_DLL_24_30	24 - 30 MHz	120.0	120.0	120.0	µs
Using CLKFX outputs	LOCK_FX_MIN		10.0	10.0	10.0	ms
	LOCK_FX_MAX		10.0	10.0	10.0	ms
Additional lock time with fine-phase shifting	LOCK_DLL_FINE_SHIFT		50.0	50.0	50.0	µs
Fine-Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.0	10.0	10.0	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.0	30.0	30.0	ps
	DCM_TAP_MAX		60.0	60.0	60.0	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Frequency Synthesis

Table 40: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross Reference

Table 41: **Parameter Cross Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II source-synchronous transmitter and receiver data-valid windows.

Table 42: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Duty Cycle Distortion(1)	T_{DCD_CLK0}	All	140	140	140	ps
	T_{DCD_CLK180}	All	50	50	50	ps
Clock Tree Skew(2)	T_{CKSKEW}	XC2V40	TBD	50	TBD	ps
		XC2V80	TBD	50	TBD	ps
		XC2V250	TBD	50	TBD	ps
		XC2V500	TBD	50	TBD	ps
		XC2V1000	TBD	80	TBD	ps
		XC2V1500	TBD	80	TBD	ps
		XC2V2000	TBD	100	TBD	ps
		XC2V3000	TBD	100	TBD	ps
		XC2V4000	TBD	TBD	TBD	ps
		XC2V6000	TBD	500	TBD	ps
		XC2V8000	TBD	TBD	TBD	ps

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
   T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O.
   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 43: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2V1000 / FF896	130	ps
		XC2V3000 / FF1152	115	ps
		XC2V3000 / BF957	130	ps
		XC2V4000 / FF1152	130	ps
		XC2V4000 / FF1517	200	ps
		XC2V4000 / BF957	140	ps
		XC2V6000 / FF1152	90	ps
		XC2V6000 / FF1517	105	ps
		XC2V6000 / BF957	105	ps

Notes:

1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 44: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Sampling Error at Receiver Pins(1)	T_{SAMP}	XC2V40	TBD	500	TBD	ps
		XC2V80	TBD	500	TBD	ps
		XC2V250	TBD	500	TBD	ps
		XC2V500	TBD	500	TBD	ps
		XC2V1000	TBD	500	TBD	ps
		XC2V1500	TBD	500	TBD	ps
		XC2V2000	TBD	500	TBD	ps
		XC2V3000	TBD	500	TBD	ps
		XC2V4000	TBD	500	TBD	ps
		XC2V6000	TBD	500	TBD	ps
		XC2V8000	TBD	TBD	TBD	ps

Notes:
1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.

Table 45: **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}	XC2V40	TBD	TBD	TBD	ns
		XC2V80	TBD	TBD	TBD	ns
		XC2V250	TBD	TBD	TBD	ns
		XC2V500	TBD	TBD	TBD	ns
		XC2V1000	TBD	0.2/0.5	TBD	ns
		XC2V1500	TBD	TBD	TBD	ns
		XC2V2000	TBD	TBD	TBD	ns
		XC2V3000	TBD	0.2/0.5	TBD	ns
		XC2V4000	TBD	TBD	TBD	ns
		XC2V6000	TBD	0.2/0.6	TBD	ns
		XC2V8000	TBD	TBD	TBD	ns

Notes:
1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the **Source-Synchronous Switching Characteristics** section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$T_X = \text{Data Period} - [\text{Jitter}^{(1)} + \text{Duty Cycle Distortion}^{(2)} + \text{TCKSKEW}^{(3)} + \text{TPKGSKEW}^{(4)}]$$

Notes:

1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the **DCM Timing Parameters** section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 42.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Virtex-II Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [\text{TSAMP}^{(1)} + \text{TCKSKEW}^{(2)} + \text{TPKGSKEW}^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections.
01/25/01	1.3	• The data sheet was divided into four modules (per the current style standard). • Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Table 18, "Delay Measurement Methodology"
04/23/01	1.5	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Added T_{REG32} symbol to Table 23. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

Date	Version	Revision
07/30/01	1.6	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Added values to the **Virtex-II Pin-to-Pin Output Parameter Guidelines** and **Virtex-II Pin-to-Pin Input Parameter Guidelines** tables. • Added **Frequency Synthesis** table.
10/02/01	1.7	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Updated the speed grade designations used in data sheets, and added Table 13, which shows the current speed grade designation for each device.
10/05/01	1.8	• Corrected the speed grade designation for the XC2V1000 device in Table 13.
10/12/01	1.9	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables.
11/28/01	2.0	• Updated values in Table 3, Table 4, Table 5, **Virtex-II Performance Characteristics**, and **Virtex-II Switching Characteristics** tables.
01/03/02	2.1	• Updated values in **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables, based on values extracted from speeds file version 1.96. • Changed the speed grade designation for the XC2V6000 device in Table 13.
07/16/02	2.2	• Updated values in Table 4, "**Quiescent Supply Current**." • Updated values in **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables, based on values extracted from speeds file version 1.111. • Added **Enhanced Multiplier Switching Characteristics** section. • Added footnote to Table 34, "**Global Clock Setup and Hold for LVTTL Standard, Without DCM**." • Added **Source-Synchronous Switching Characteristics** section.
09/26/02	2.3	• Removed mention of MIL-M-38510/605 specification. • Added footnotes to Table 2 and Table 6.
12/06/02	2.4	• Revised SSTL2 values in Table 6 to match the latest JEDEC specification. • Added footnote regarding V_{IN} PCI compliance to Table 1. • Added footnote regarding CLKOUT_DUTY_CYCLE_DLL to Table 38.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- **Virtex™-II Platform FPGAs: Introduction and Overview (Module 1)**
- **Virtex™-II Platform FPGAs: Detailed Description (Module 2)**
- **Virtex™-II Platform FPGAs: DC and Switching Characteristics (Module 3)**
- **Virtex™-II Platform FPGAs: Pinout Information (Module 4)**