TECHNICAL NOTE

SYNCHRONOUS TIMING FOR DDR SDRAM

INTRODUCTION

The rapid deployment of DDR SDRAM is raising an interesting issue with data capture. Case in point, there are FBGA controllers which do not utilize the data strobe (DQS) during READ operations. These controllers are capturing the read sequences in the clock domain. This data capture scheme is causing some confusion when the data sheets reference a read data timing spec from the data strobe. The intent of this document is to provide a better explanation of synchronous timing of DDR SDRAM in relative read data capture.

SINGLE DQ

Capturing read data synchronously from DDR SDRAM devices raises a set of problems that are not addressed in data sheets. The best place to start is with a single DQ pin. In this explanation we will use a 2 Meg x 32 device and start with DQ7. For the purpose of this explanation, let us assume DQ7 has a ^{t}AC of 0 with a 50/50 ^{t}CK under all condition. The data valid window (DVW) for this DQ is determined by the half clock cycle or 5ns with a 10ns clock. (See Figure 1.)

In a real world environment, the worst case half cycle would have to be used to determine the data valid for a particular DQ.

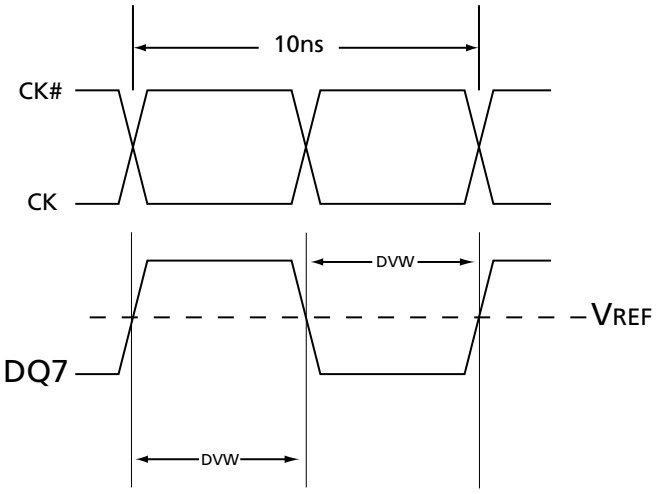

Figure 1
Single DQ

MULTIPLE DQs

For read data capture, the data valid window needs to compensate for variations over process and environment for mulitple DQs. The skew from DQ to DQS (^{t}DQSQ) does not factor in when running the parts synchronously. The device specification shows data must be valid between the ^{t}AC (MIN) and ^{t}AC (MAX) for a given clock cycle regardless of the components DQ skew. The only timing components that are relevant in determining the DVW in this case are ^{t}AC and ^{t}CK. Data will be valid for ½ ^{t}CK – ^{t}AC (MAX) + ^{t}AC (MIN)

Example:
^{t}CK = 10ns
^{t}AC(MAX) = 750ps
^{t}AC (MIN) = -750ps

DVW = 5ns – 750ps + -750ps = 3.5ns

The DVW takes into consideration both worst case ^{t}AC parameters for all DQs over temperature and voltage. Note, this is not the amount of time for one DQ to be valid in relation to the clock but all of the DQs. To calculate worst case setup and hold time, ^{t}AC(MAX) and ^{t}AC (MIN) are to be used to determine the timing budget. Figure 2 illustrates all DQs in relation to the crossing of CK and CK#.

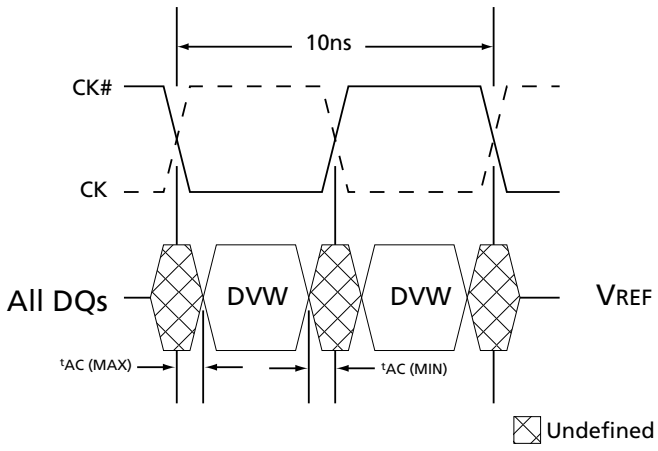

Figure 2
Multiple DQs

DATA CAPTURE

There are several ways to perform a data capture using the controller. The two most prevalent methods are to use either a quarter clock or half clock for the DDR SDRAM controller. The controller will run an internal clock at four times the frequency of the DDR clock and use the rising edge to capture data with the quarter clock scheme, as shown in Figure 3. The half clock scheme works in a similar fashion with the internal controller clock running at two times the DDR clock rate, also using the rising edge to latch data, as shown in Figure 4. However, the half clock scheme can be misleading due to the negative hold times that are inherent to this type of design.

SETUP TIME

Note that the setup time is calculated with ^{t}AC (MAX) and ½ ^{t}CK in relation the DRAM, not the controller. Subtracting ^{t}AC (MAX) from ½ ^{t}CK will provide worst case setup time at the DRAM, in relation to the desired clock edge for all DQs on the bus. Also note that the signal flight time and clock skew must be accounted for on the controller side to align the half clock or quarter clock delay in the controller.

HOLD TIME

The hold time is calculated with ^{t}AC (MIN). DDR parts guarantee data to be valid up to ^{t}AC (MIN) for all DQs of the falling edge of the DDR clock. The PCB flight time and clock jitter will shift this, and must be accounted for. As mentioned previously, if the controller is using a half clock scheme to latch data the hold time in most cases will be negative.

SUMMARY

The main point to remember when developing a timing budget for synchronous read data capture is the only DDR SDRAM timing parameters required are ^{t}AC(MIN) and ^{t}AC(MAX). From these two parameters, the data valid window at the pin of the DDR device can be determined. The data valid window size will not change, but it will shift in relation to clock depending PCB trace length. By adding a delay to the clock and clock bar, the window can achieve additional hold time if needed. However, adding this delay to clock and clock bar will also shift the data valid window for the WRITE commands and needs to be considered while developing the read data capture timing budget.

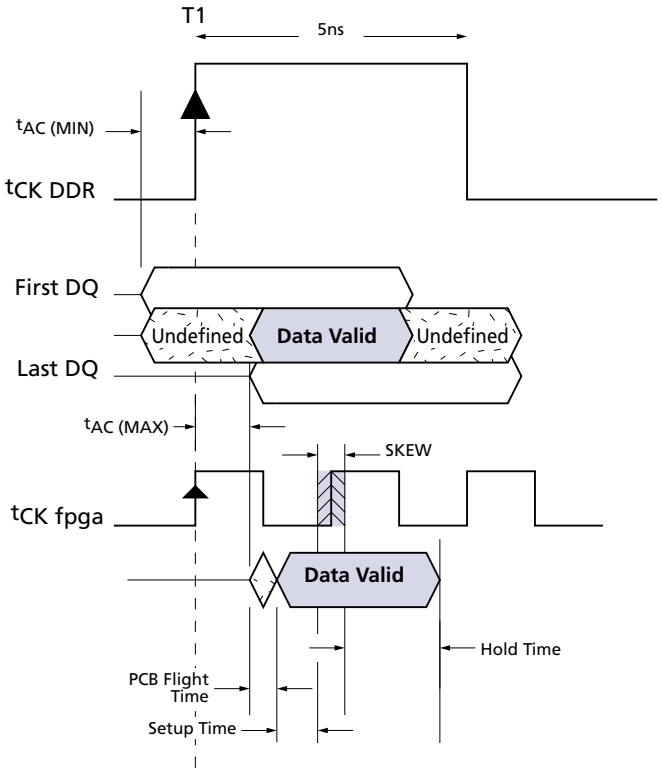

Figure 3
Quarter Clock

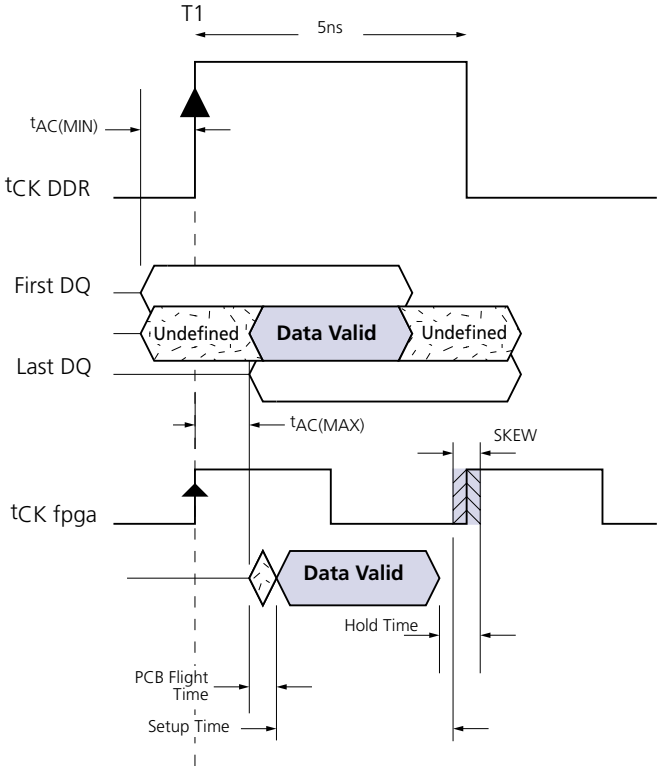

Figure 4
Half Clock

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